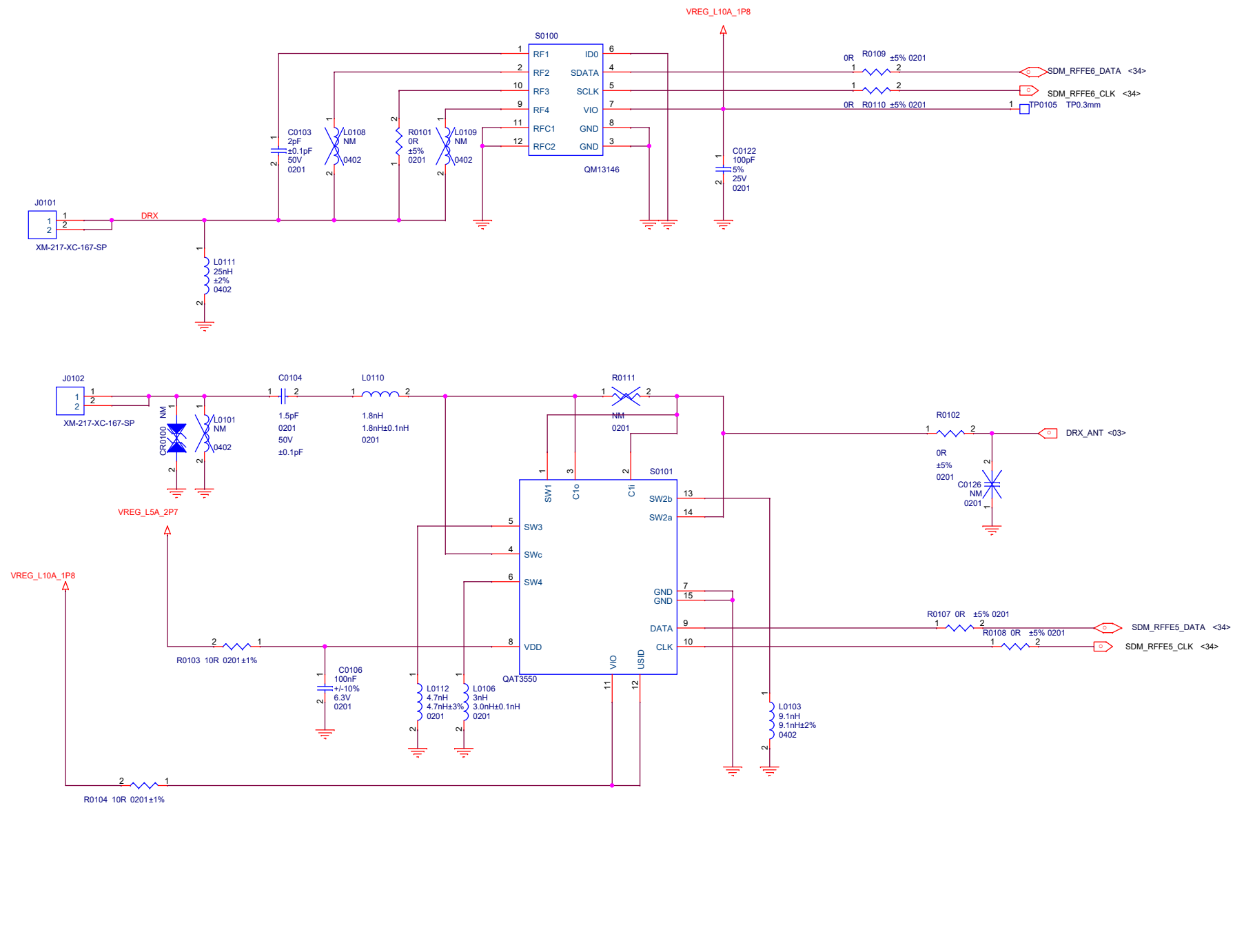


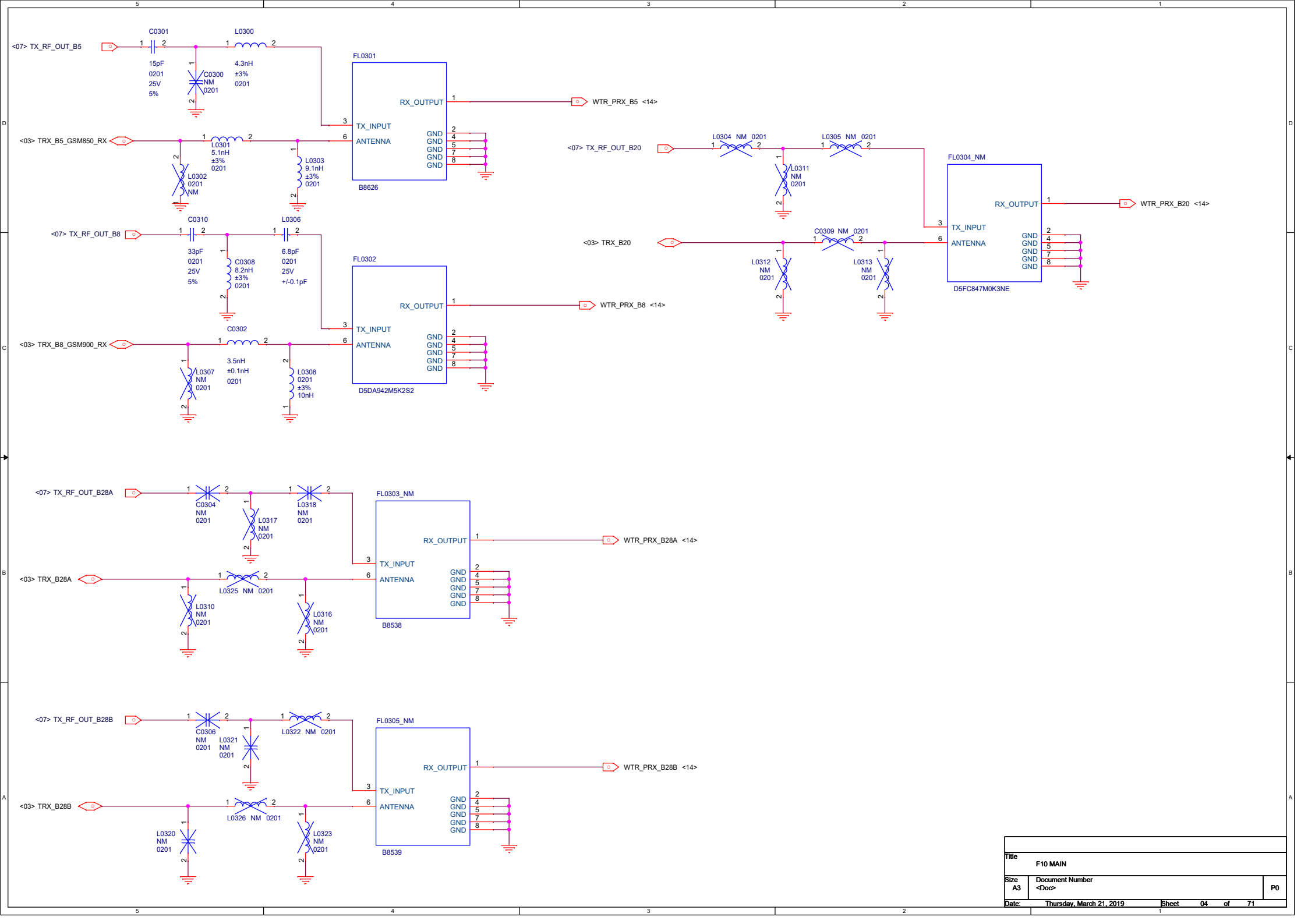
	5	4	3	2	1
D					
C					
B					
A					

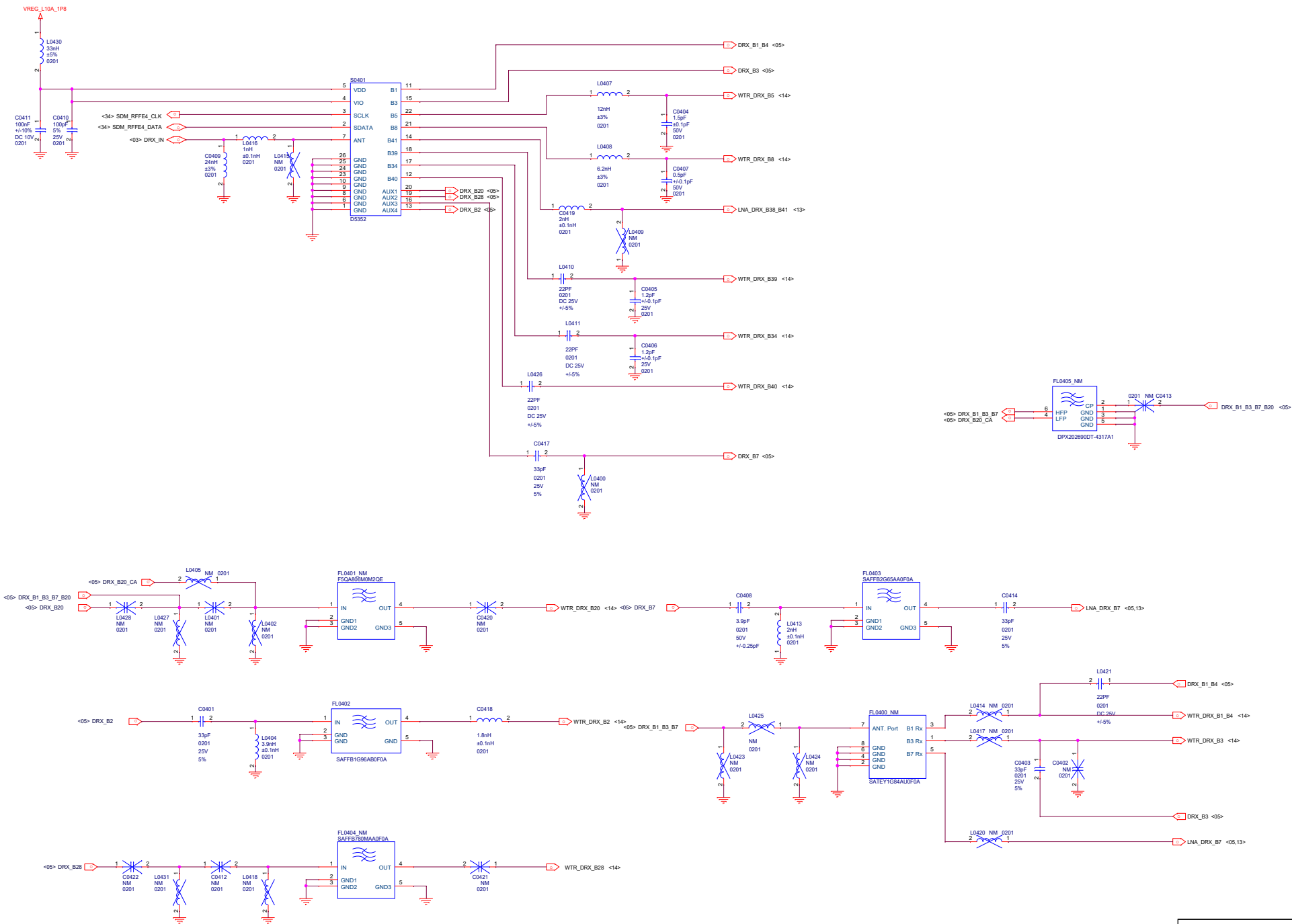
Title		F10 MAIN	
Size	A2	Document Number	CONTENT
Date:	Thursday, March 21, 2019	Sheet	01 of 71

DRX ANT



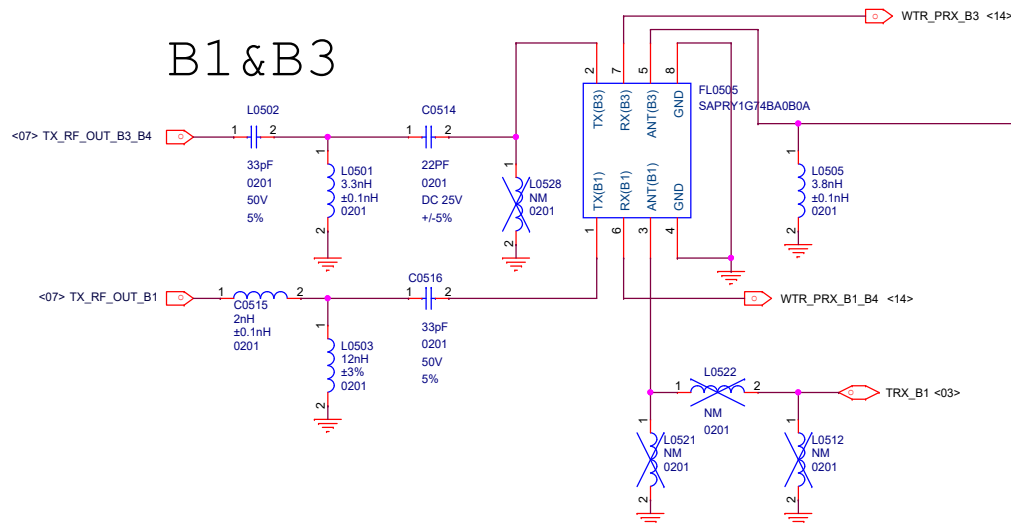
Title				
F10 MAIN				
Size	Document Number			P0
A3	<Doc>			
Date:	Thursday, March 21, 2019		Sheet	02 of 71



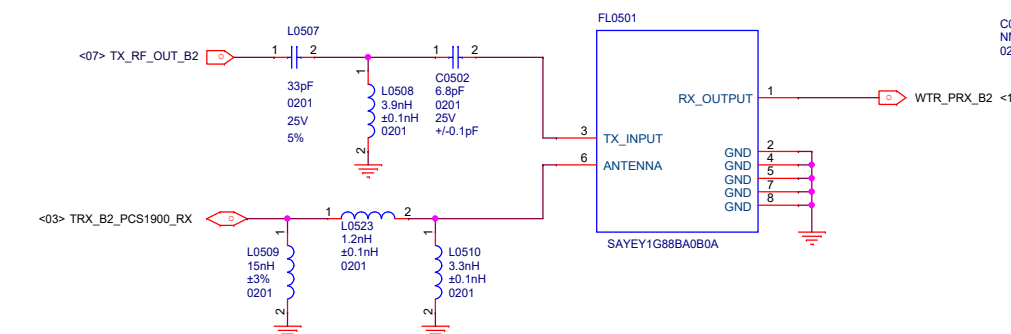


Title		F10 MAIN
Size		Document Number
A2		<Doc>
Date	Thursday, March 21, 2019	Sheet 06 of 71

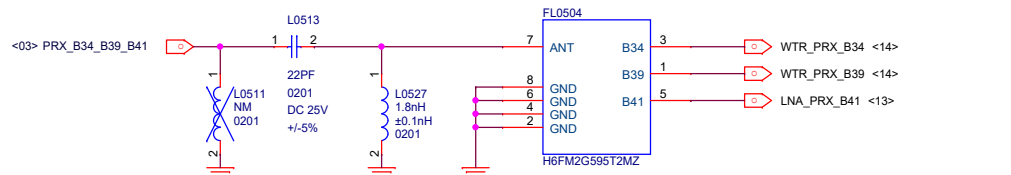
B1&B3



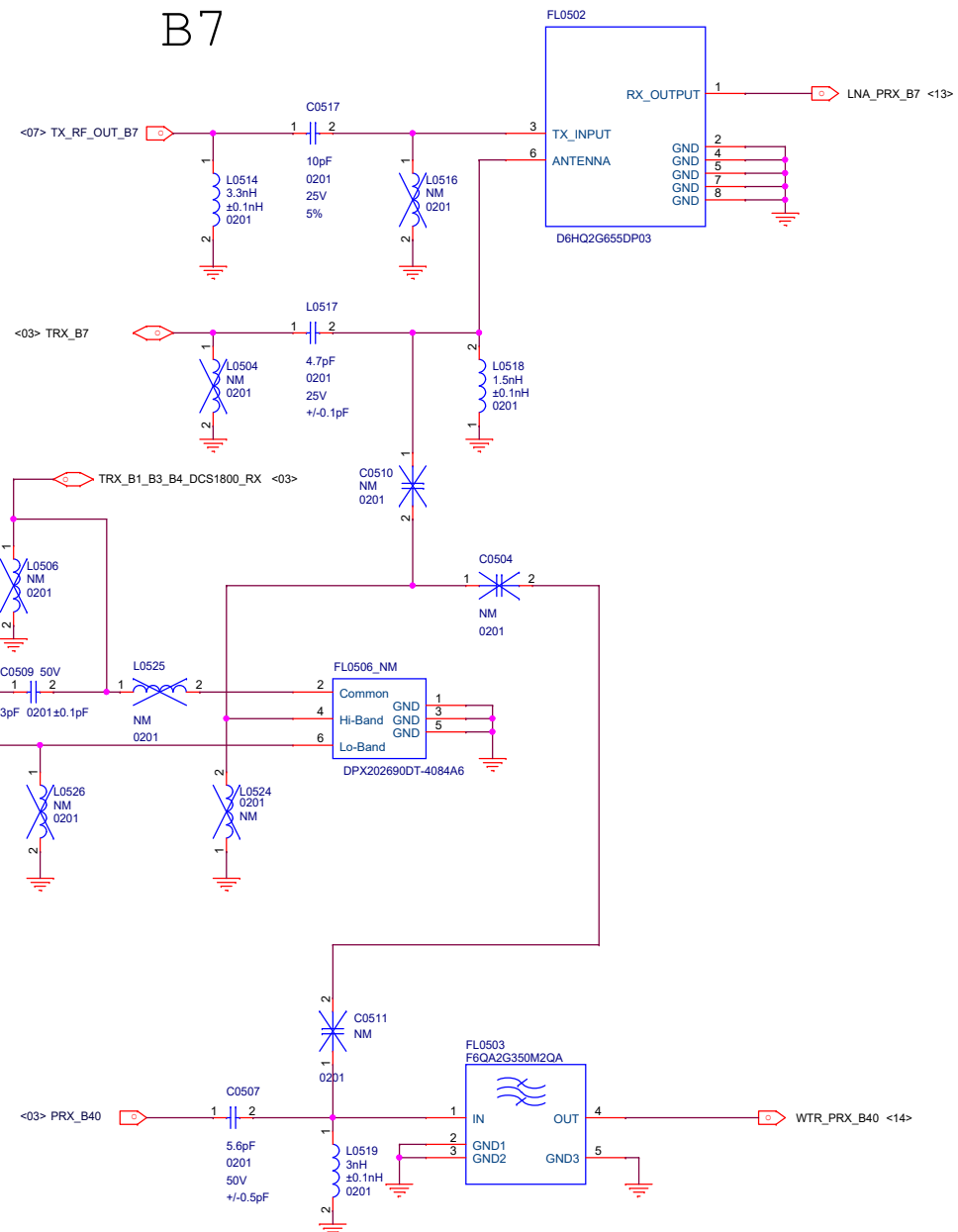
B2



PRX B34_B39_B41



B7





5

4

3

2

1

D

D

C

C

B

B

A

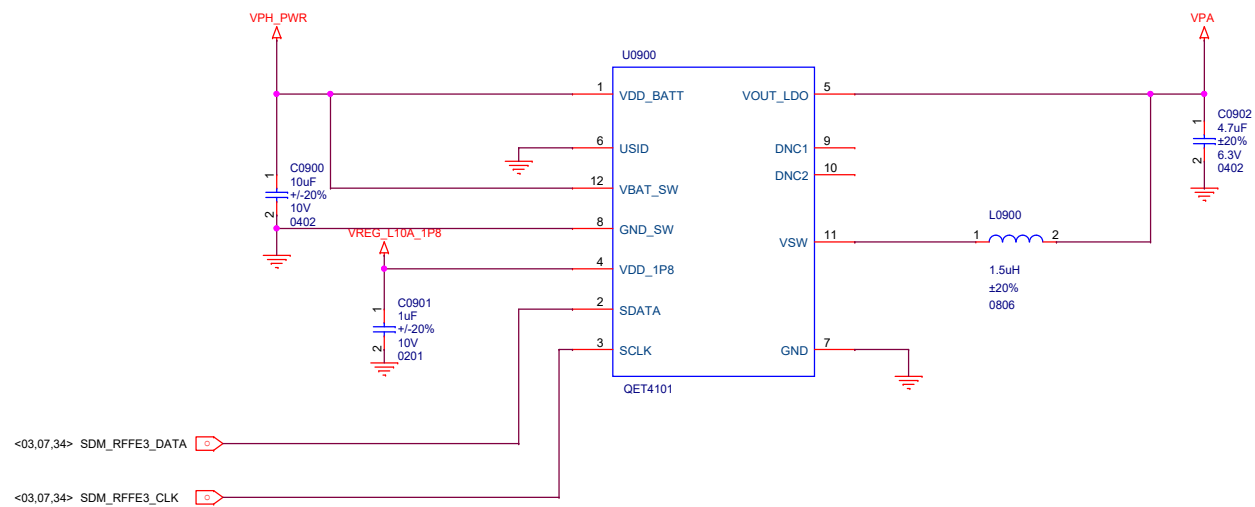
A

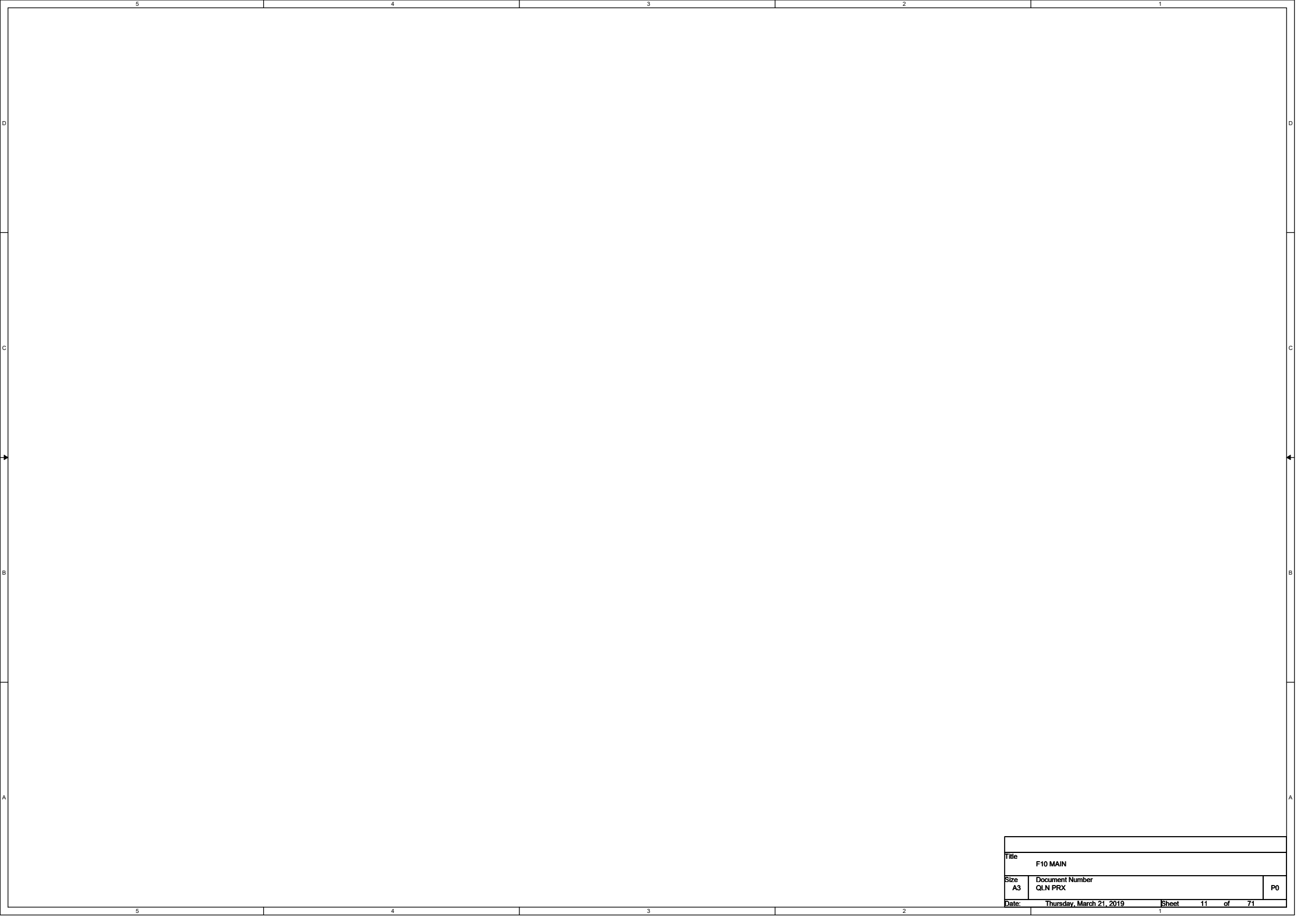
Title			
F10 MAIN			
Size	Document Number		
A3	PA2		
Date:	Thursday, March 21, 2019	Sheet	06 of 71

P0

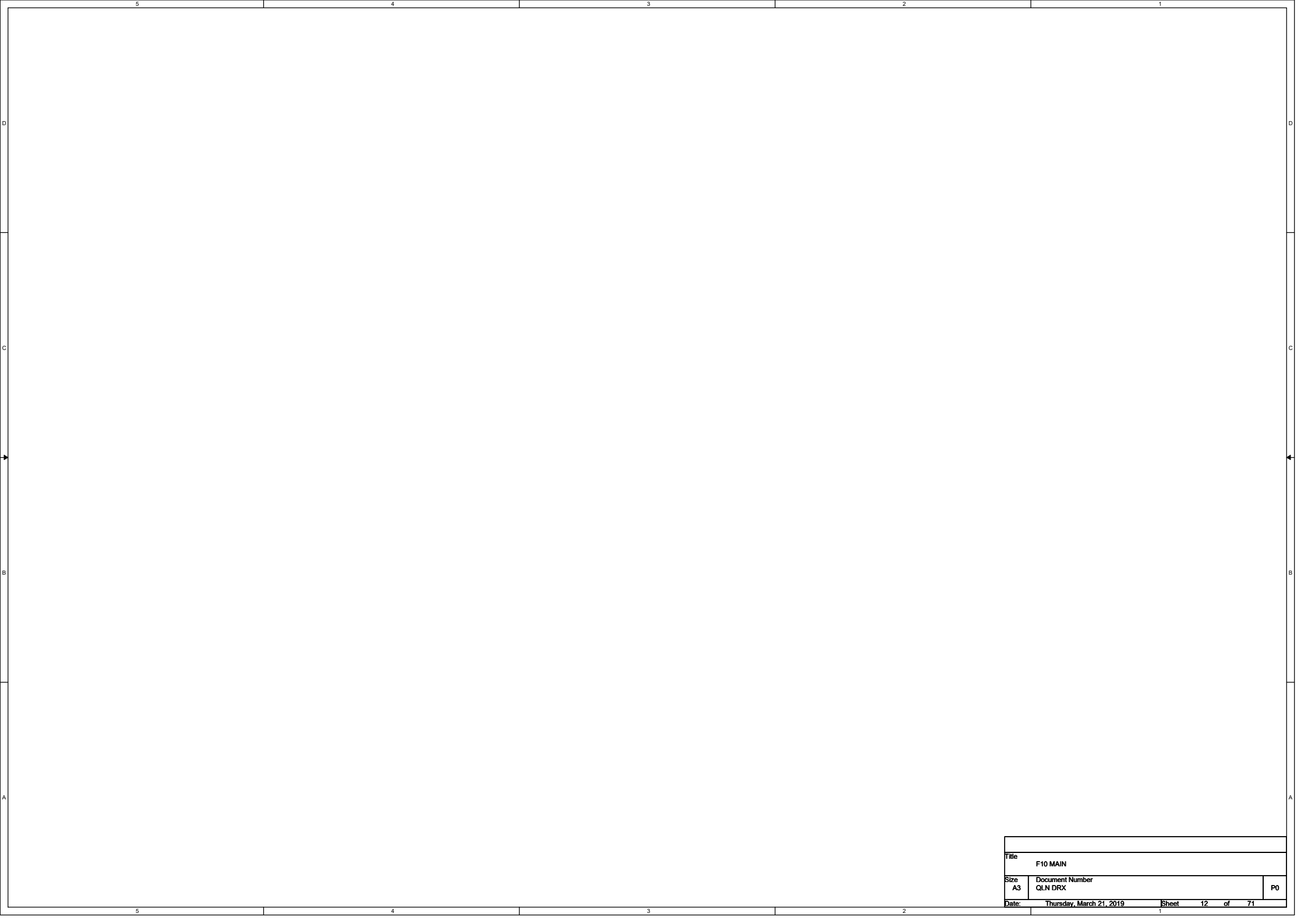
5	4	3	2	1
D				
C				
B				
A				

Title			
F10 MAIN			
Size	Document Number		
A3	Reserved(for PA)		
Date:	Thursday, March 21, 2019	Sheet	09 of 71

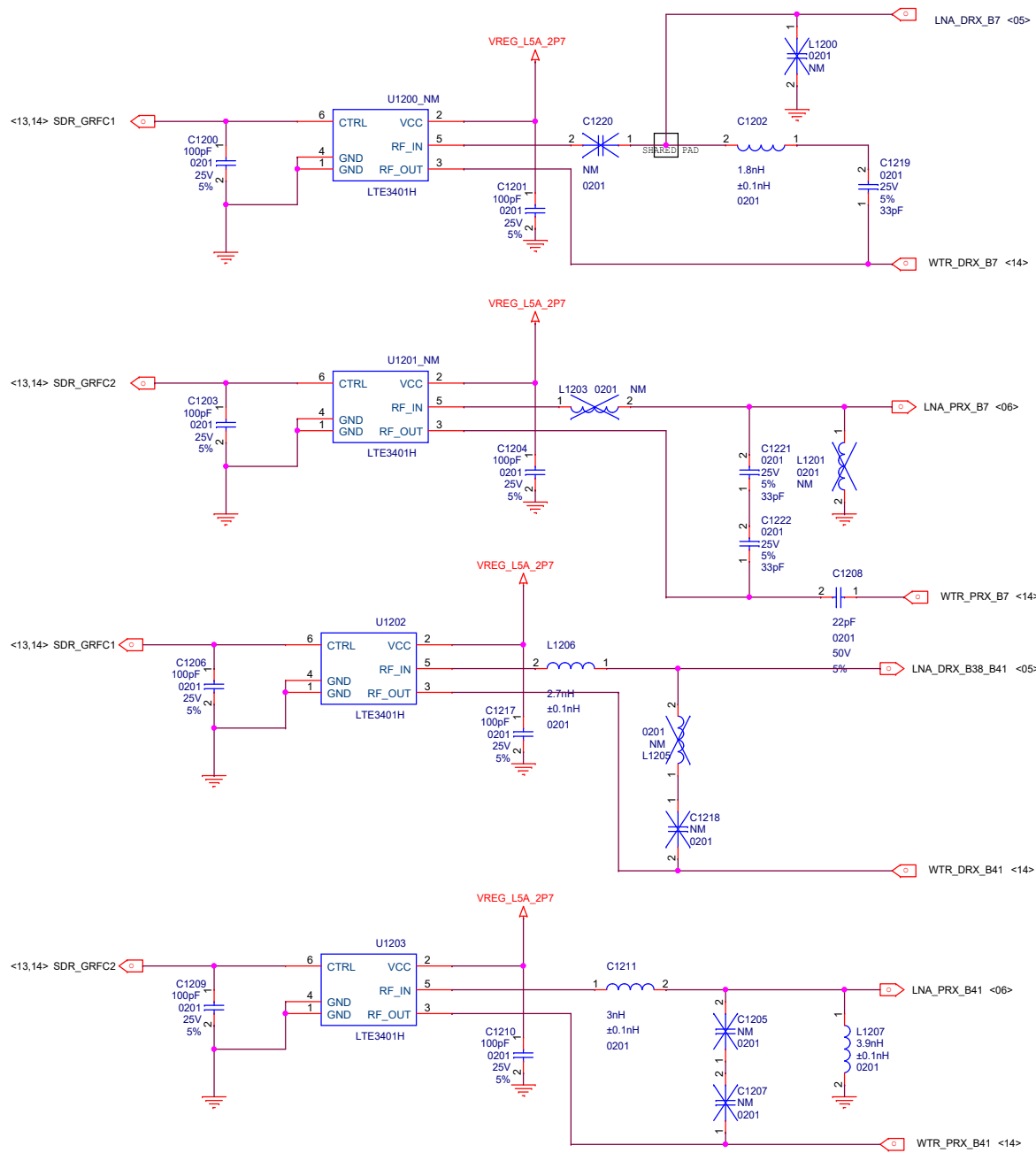


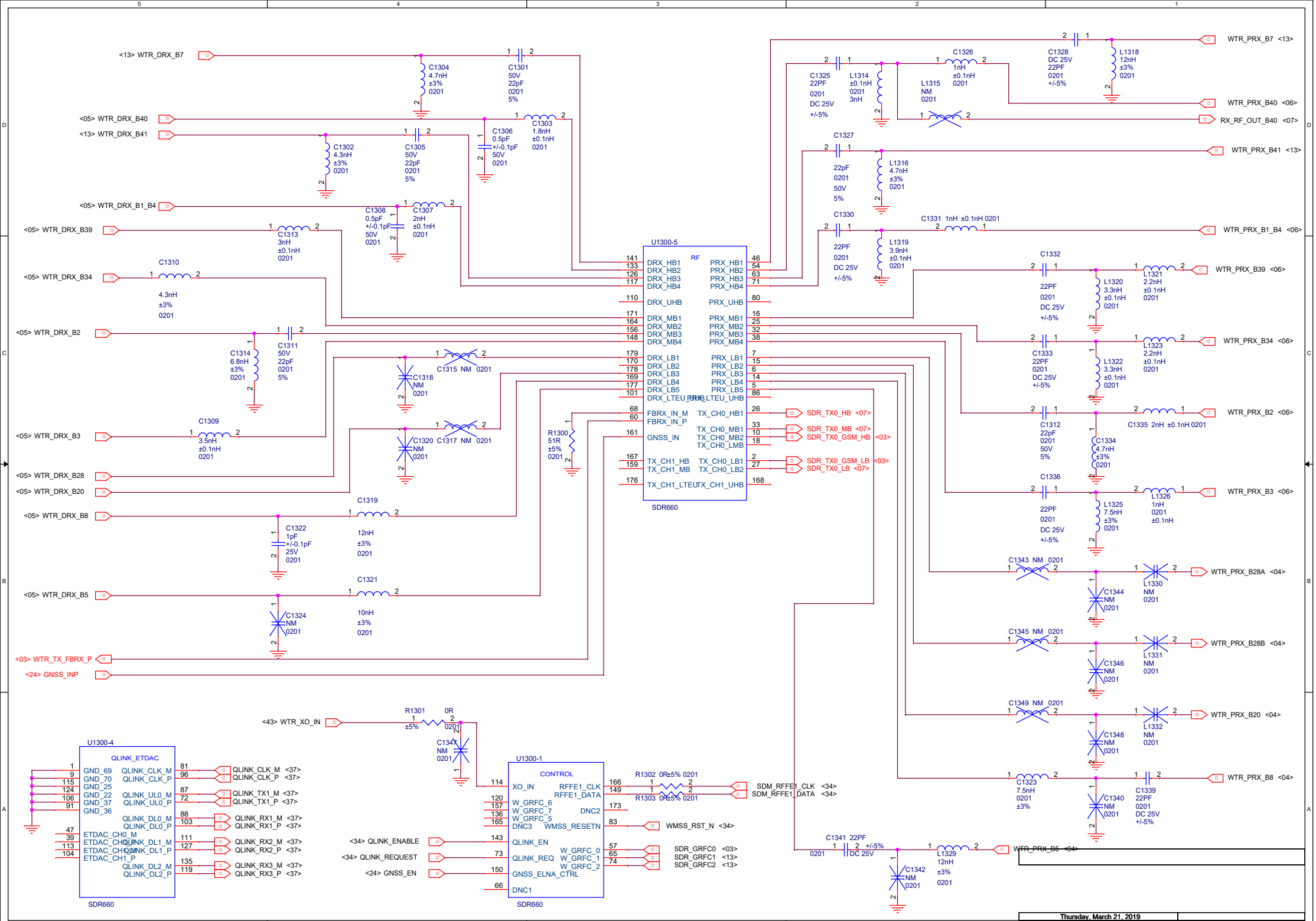


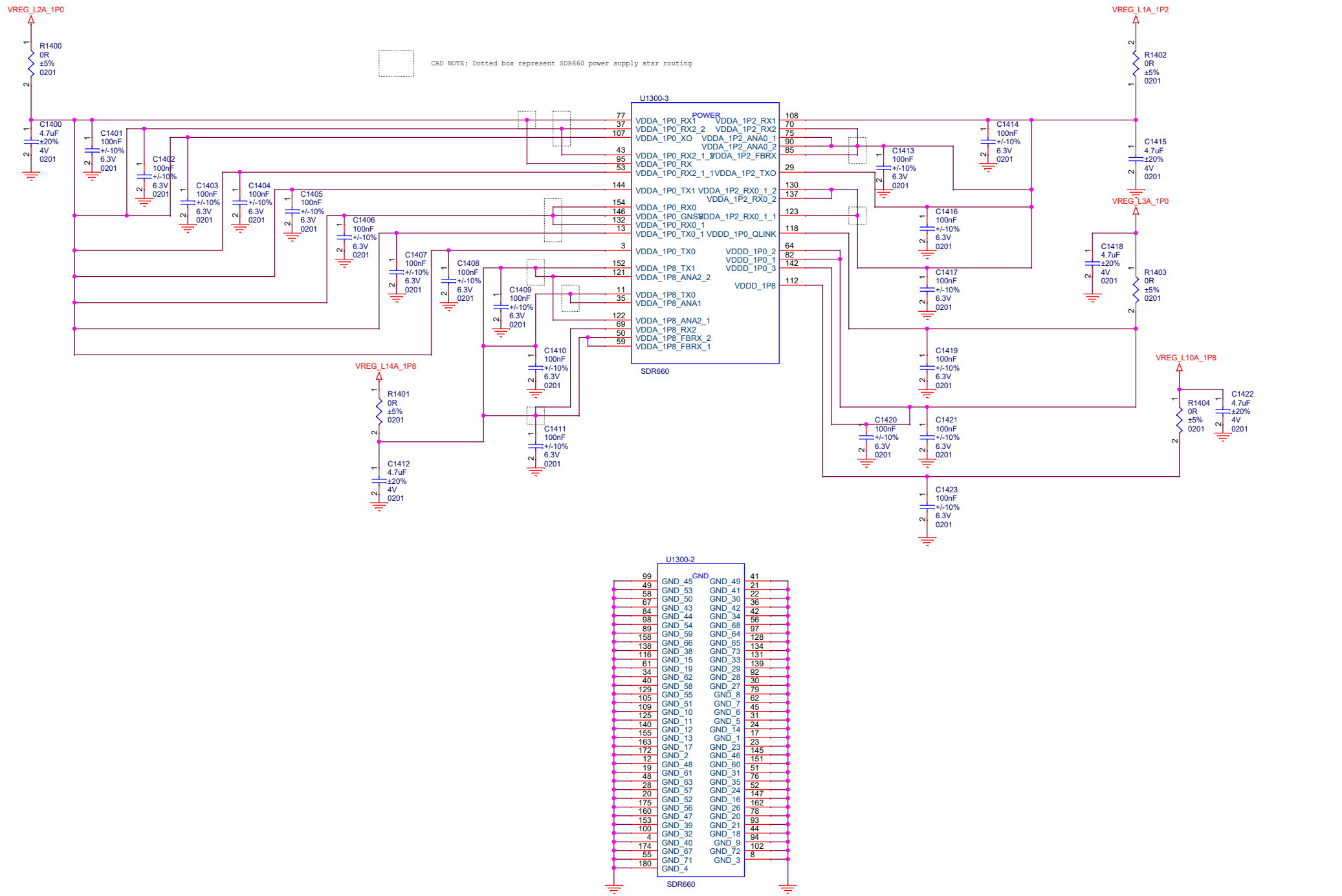
Title			
F10 MAIN			
Size	Document Number		P0
A3	QLN PRX		
Date:	Thursday, March 21, 2019	Sheet	11 of 71



Title			
F10 MAIN			
Size	Document Number		P0
A3	QLN DRX		
Date:	Thursday, March 21, 2019	Sheet	12 of 71





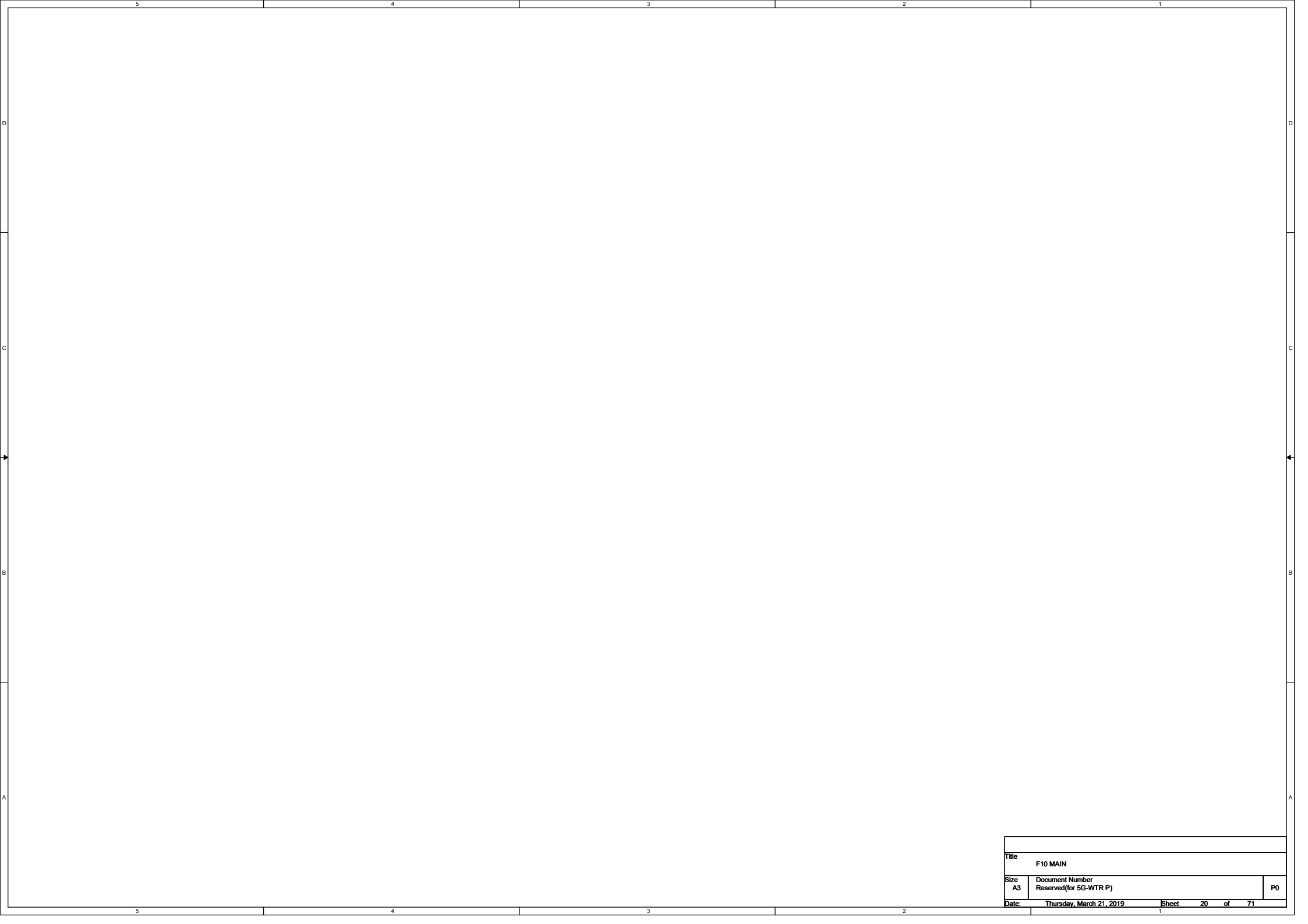


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D					
C					
B					
A					

Title		
F10 MAIN		
Size	Document Number	P0
A3	Reserved(for WTR)	
Date:	Thursday, March 21, 2019	Sheet 16 of 71

	5	4	3	2	1
D					
C					
B					
A					

Title		
F10 MAIN		
Size	Document Number	P0
A3	Reserved(for MM Wave)	
Date:	Thursday, March 21, 2019	Sheet 18 of 71



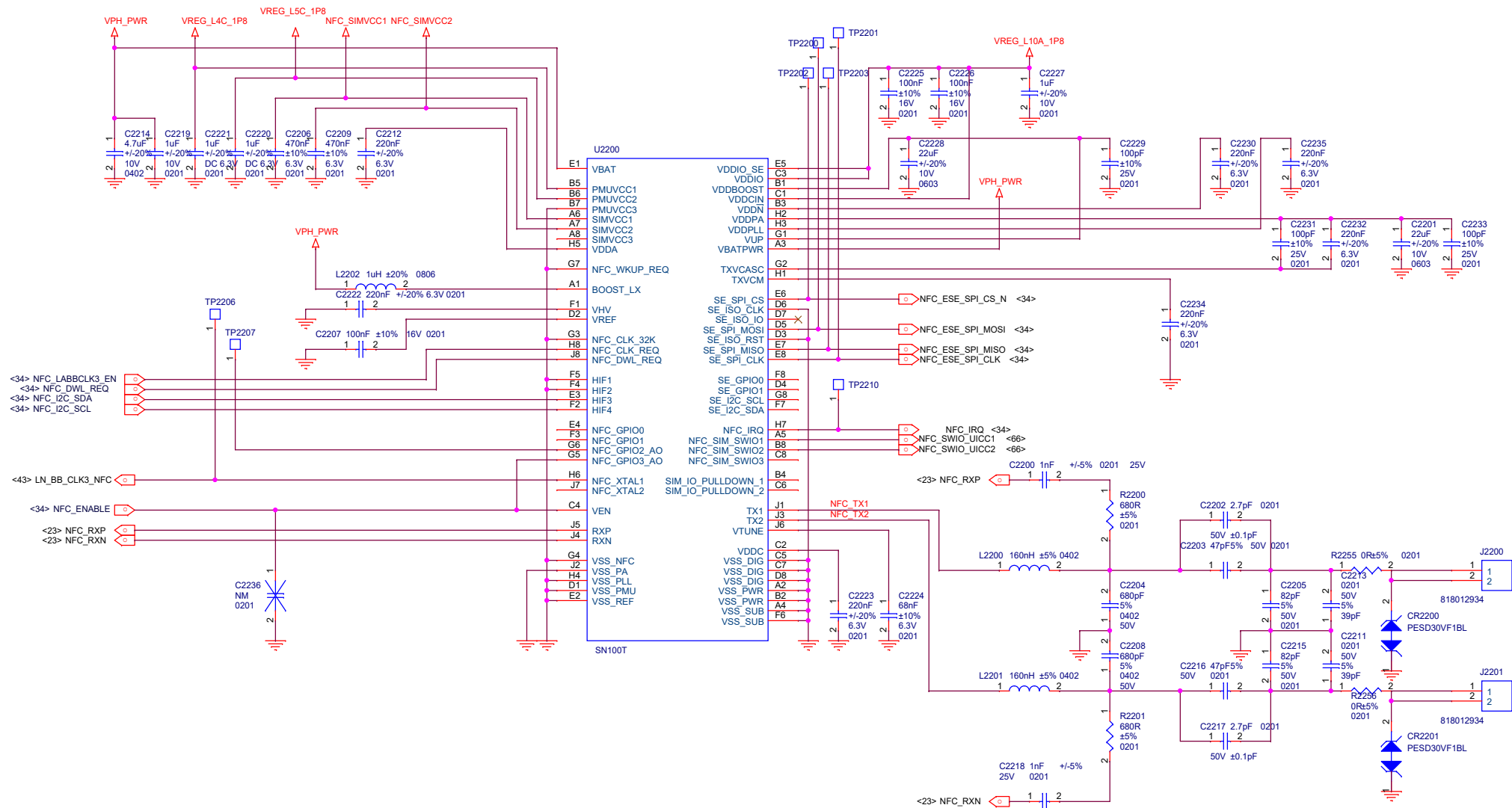
Title			
F10 MAIN			
Size	Document Number		P0
A3	Reserved(for 5G-WTR P)		
Date:	Thursday, March 21, 2019	Sheet	20 of 71

5	4	3	2	1
D				
C				
B				
A				

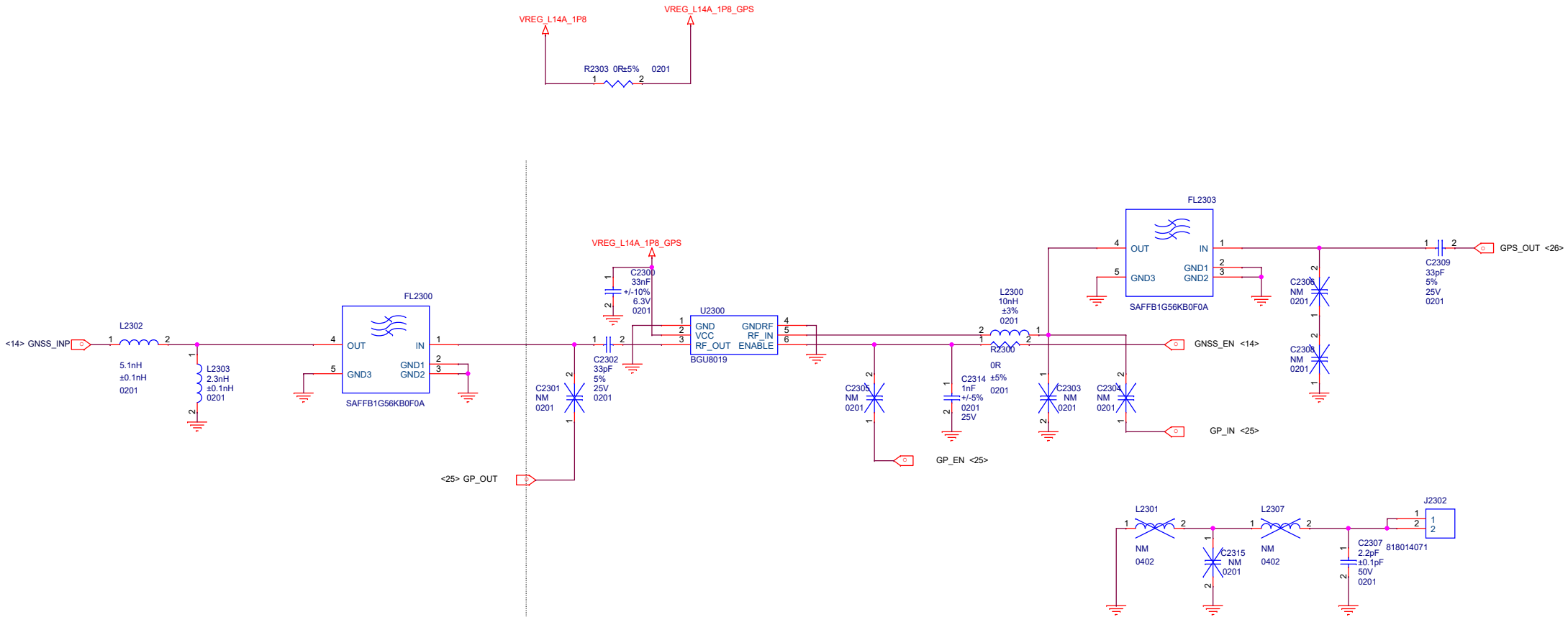
Title			
F10 MAIN			
Size	Document Number		
A3	Reserved(for 5G-DC/DC)		
Date:	Thursday, March 21, 2019	Sheet	21 of 71

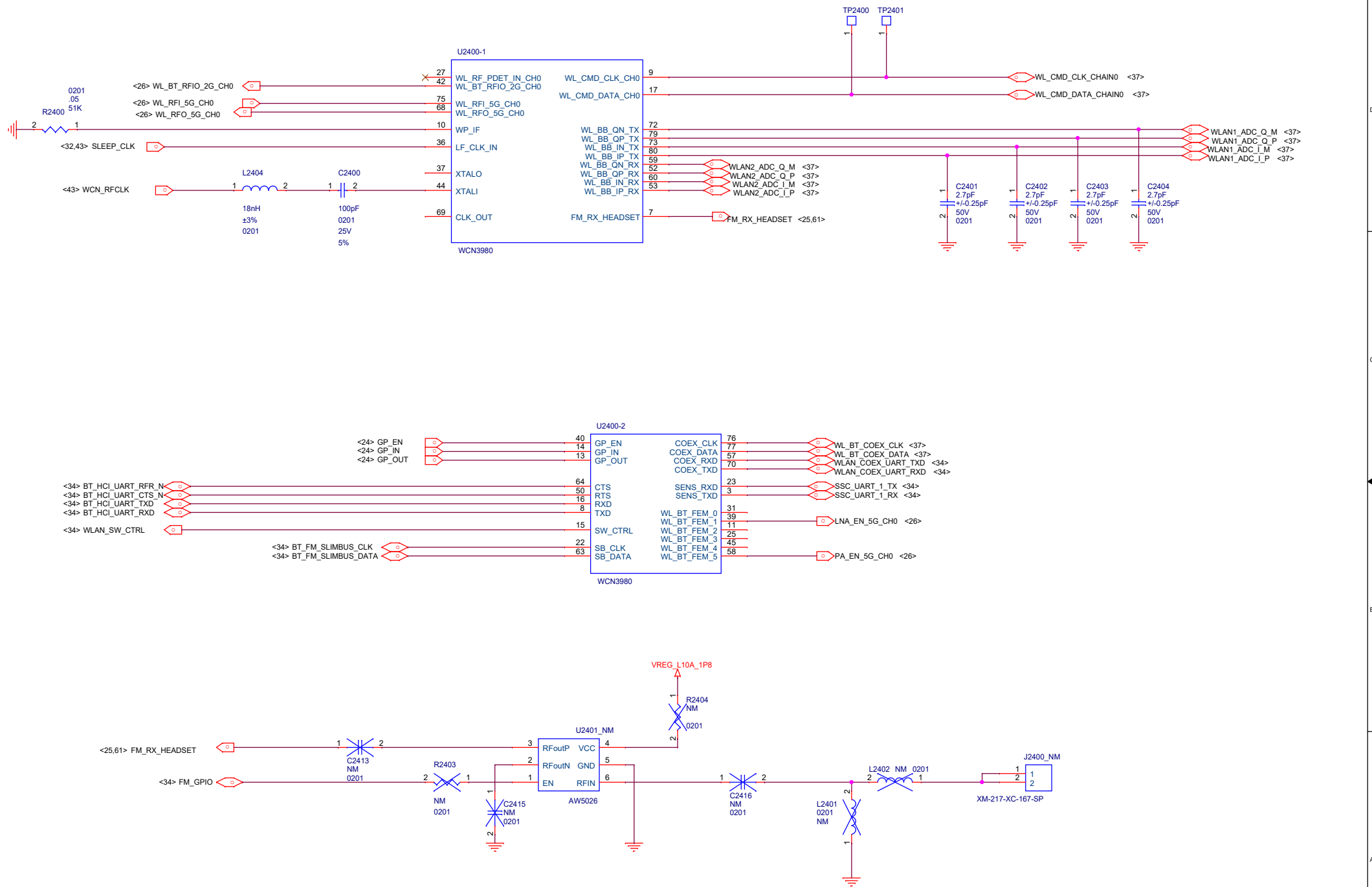
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D					
C					
B					
A					

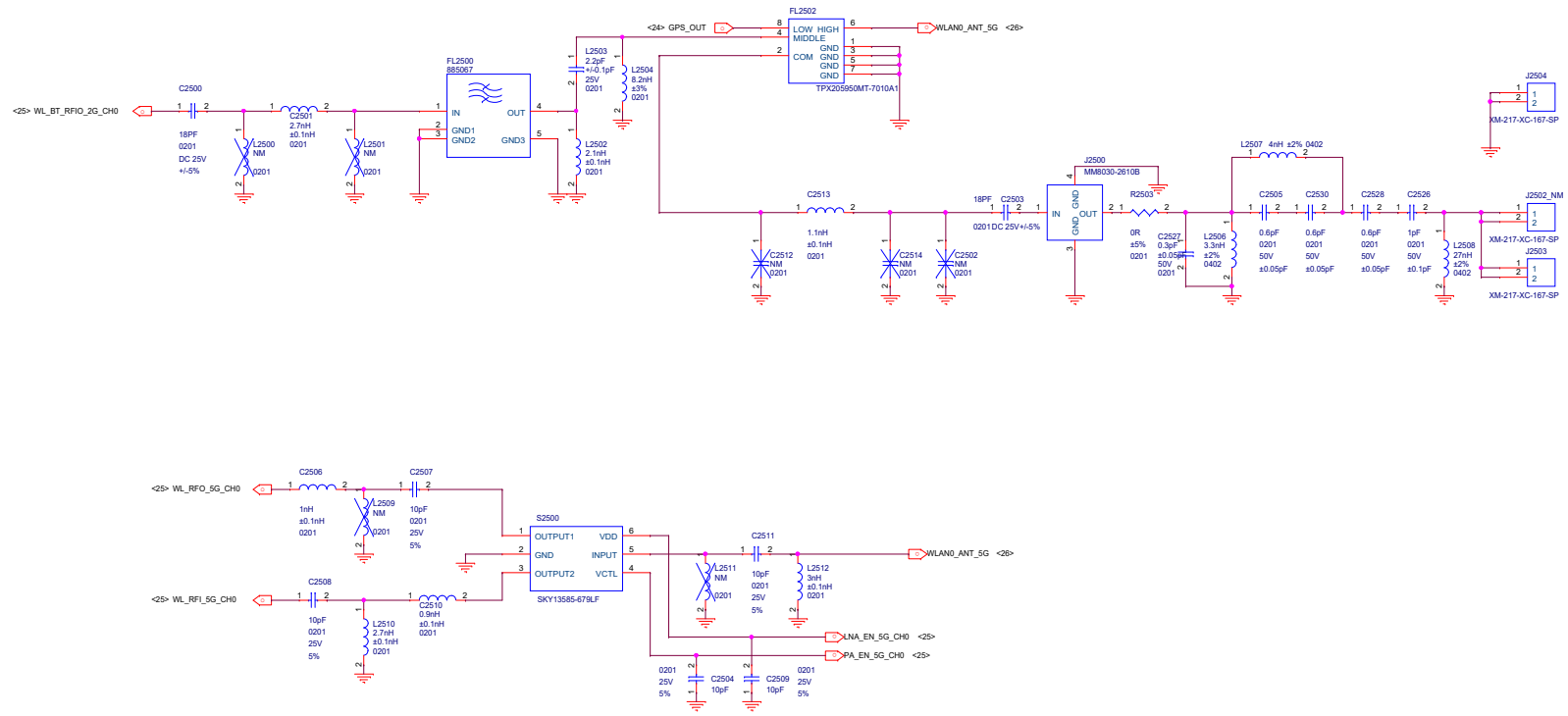
Title		
F10 MAIN		
Size	Document Number	
A3	NFC	
Date:	Thursday, March 21, 2019	Sheet 22 of 71

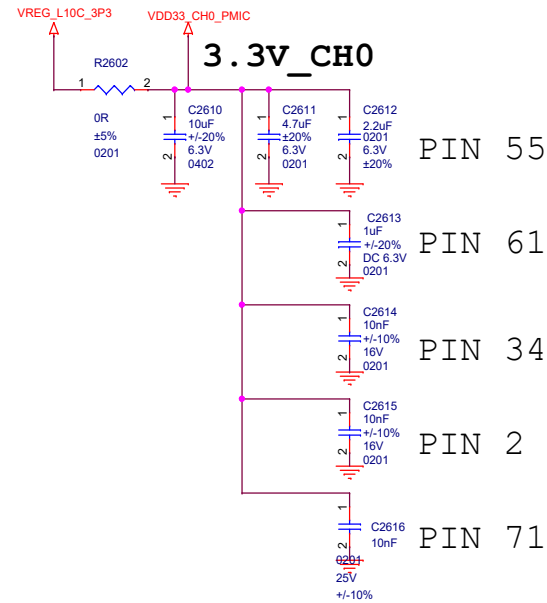
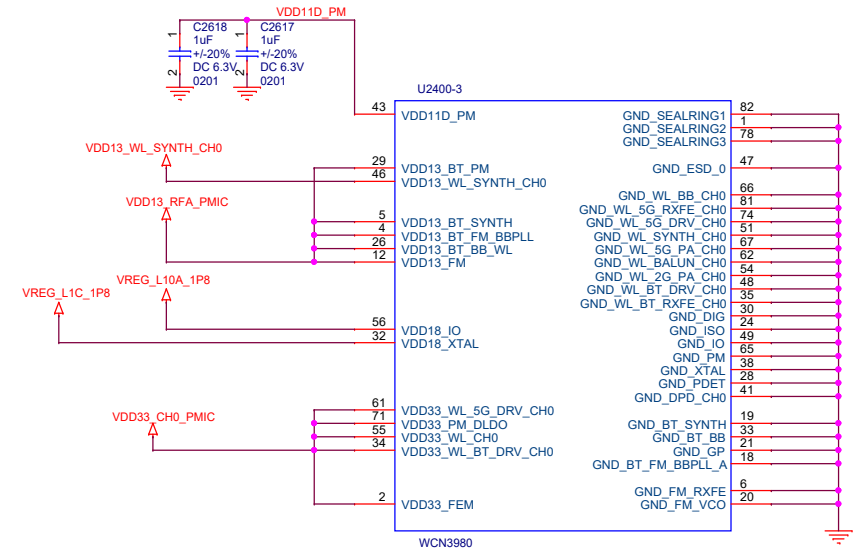
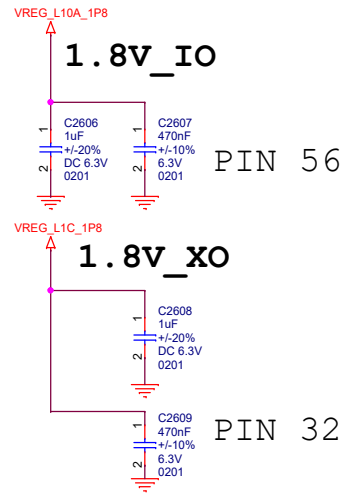
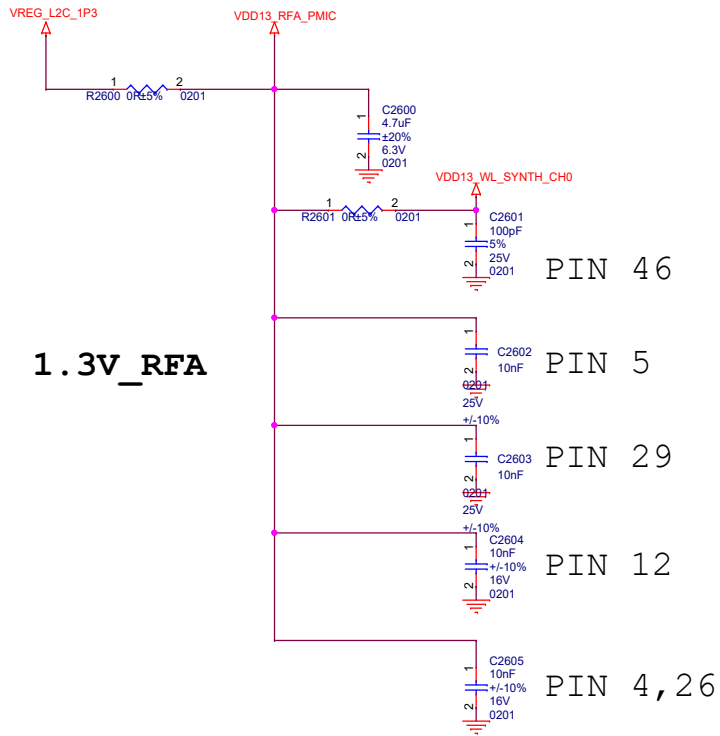


Title			
F1 MAIN			
Size	Document Number		
A3	Reserved(for PA)		
P0			
Date:	Wednesday, April 10, 2019		Sheet 23 of 71







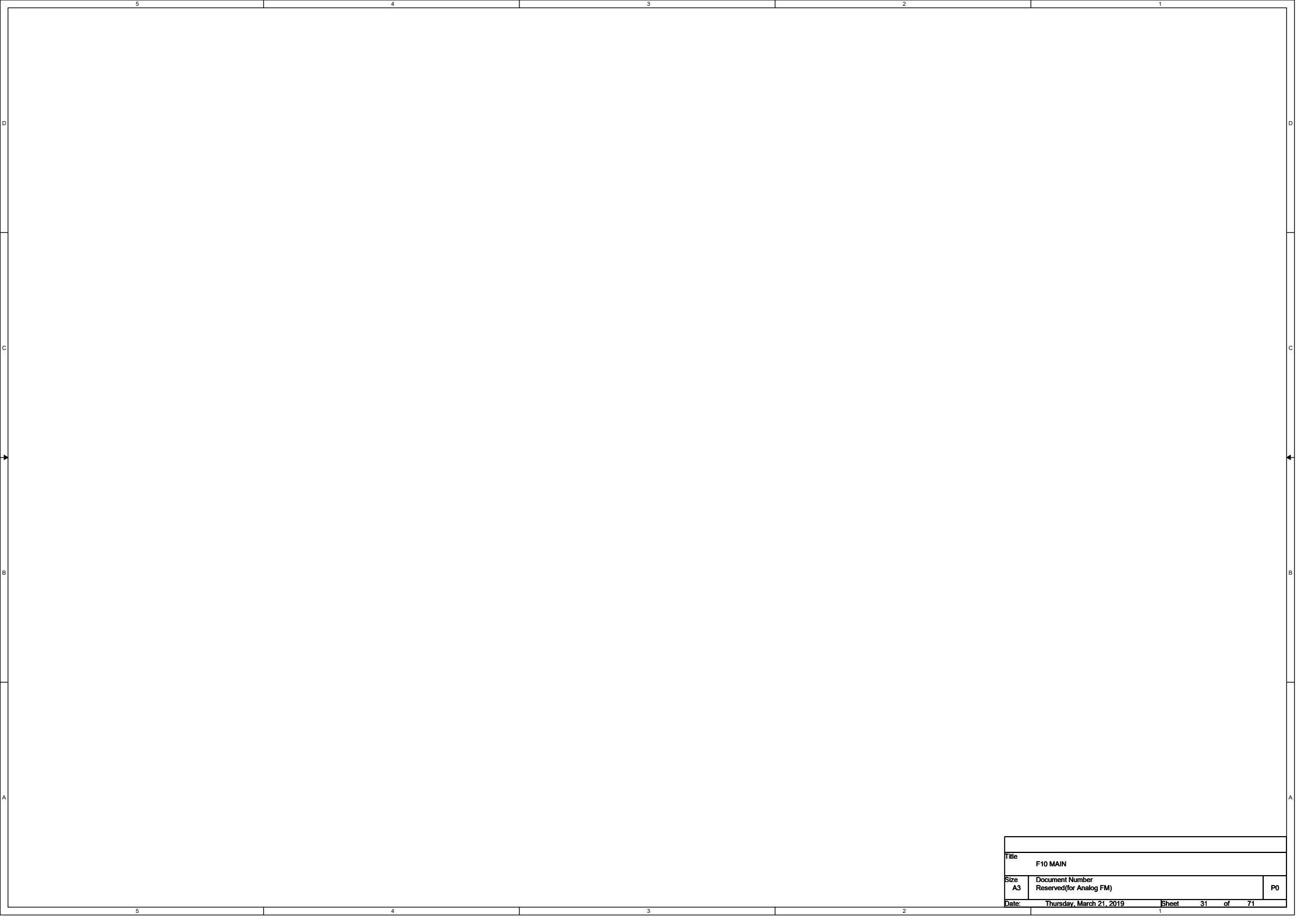


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D					
C					
B					
A					

Title		
F10 MAIN		
Size	Document Number	P0
A3	Reserved(for 11ad/11ax)	
Date:	Thursday, March 21, 2019	Sheet 29 of 71

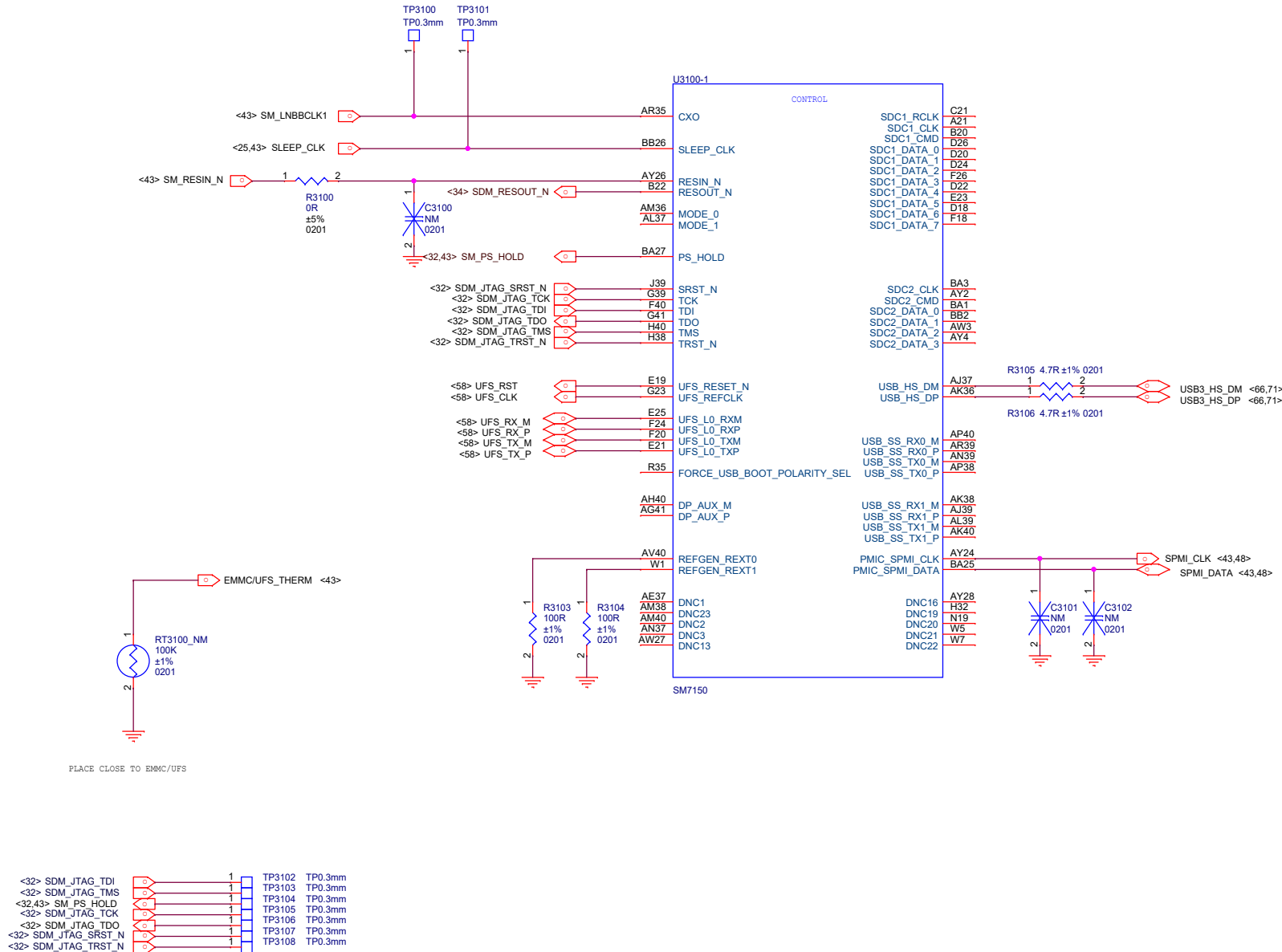
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D					
C					
B					
A					

Title			
F10 MAIN			
Size	Document Number		
A3	Reserved(for Digital FM)		
Date:	Thursday, March 21, 2019	Sheet	30 of 71

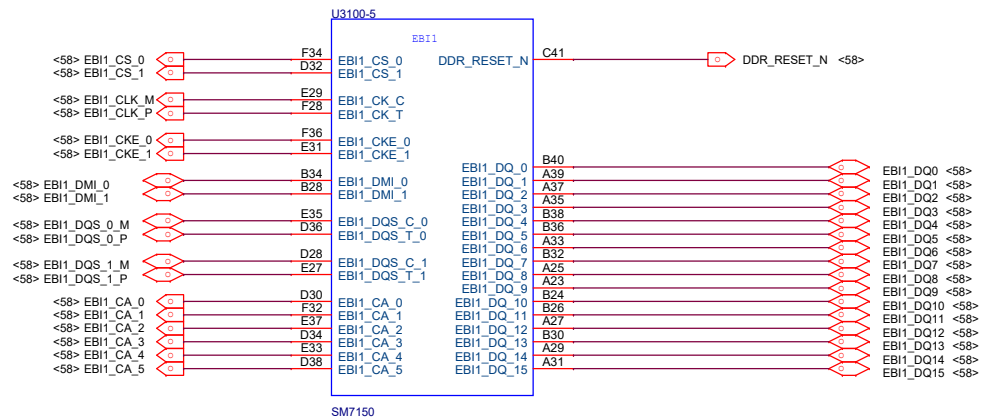
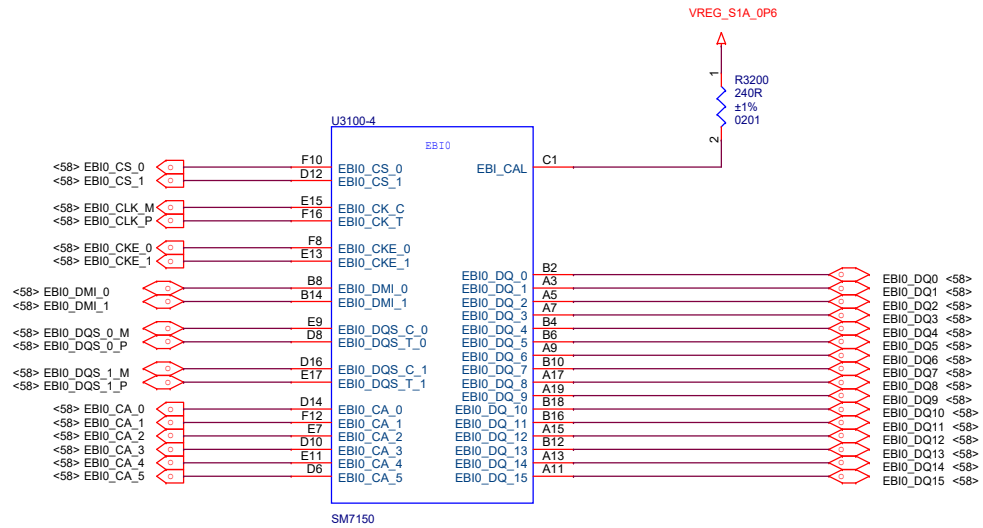


Title		
F10 MAIN		
Size	Document Number	P0
A3	Reserved(for Analog FM)	
Date:	Thursday, March 21, 2019	Sheet 31 of 71

MODE	Operation
00	NATIVE
01	TIC
10	ATEST
11	TEST



Title		
F10 MAIN		
Size	Document Number	P0
A3	SDM855 Control	
Date:	Thursday, March 21, 2019	Sheet 32 of 71



REAR CAMERA
IMX586 48M

FRONT CAMERA
S5K3T1SP 20M
ULTRA WIDE CAMERA
3P9 16M

REAR CAMERA TELE
3m5 13M

REAR CAMERA TELE
8M

FRONT- Ultra SWITCH

<67> MIPI_WIDE_CLK_P
<67> MIPI_WIDE_CLK_M
<67> MIPI_WIDE_LANE0_P
<67> MIPI_WIDE_LANE0_M
<67> MIPI_WIDE_LANE1_P
<67> MIPI_WIDE_LANE1_M
<67> MIPI_WIDE_LANE2_P
<67> MIPI_WIDE_LANE2_M
<67> MIPI_WIDE_LANE3_P
<67> MIPI_WIDE_LANE3_M
<68> MIPI_CSI1_CLK_P
<68> MIPI_CSI1_CLK_M
<68> MIPI_CSI1_LANE0_P
<68> MIPI_CSI1_LANE0_M
<68> MIPI_CSI1_LANE1_P
<68> MIPI_CSI1_LANE1_M
<68> MIPI_CSI1_LANE2_P
<68> MIPI_CSI1_LANE2_M
<68> MIPI_CSI1_LANE3_P
<68> MIPI_CSI1_LANE3_M
<69> MIPI_ULTRA_CLK_P
<69> MIPI_ULTRA_CLK_M
<69> MIPI_ULTRA_LANE0_P
<69> MIPI_ULTRA_LANE0_M
<69> MIPI_ULTRA_LANE1_P
<69> MIPI_ULTRA_LANE1_M
<69> MIPI_ULTRA_LANE2_P
<69> MIPI_ULTRA_LANE2_M
<69> MIPI_ULTRA_LANE3_P
<69> MIPI_ULTRA_LANE3_M
<67> MIPI_CSI3_CLK_P
<67> MIPI_CSI3_CLK_M
<67> MIPI_CSI3_LANE0_P
<67> MIPI_CSI3_LANE0_M
<67> MIPI_CSI3_LANE1_P
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AF6
AE5
AE7
AD6
AC5
AB4
AB6
AA5
AA7
Y6
AG5
AH6
AH4
AJ5
AK6
AL7
AL5
AM6
AM4
AN5
AF2
AG3
AG1
AH2
AJ3
AK4
AK2
AL3
AL1
AM2
AE3
AD4
AD2
AC3
AC1
AB2

U3100-6

MIPI

SM7150

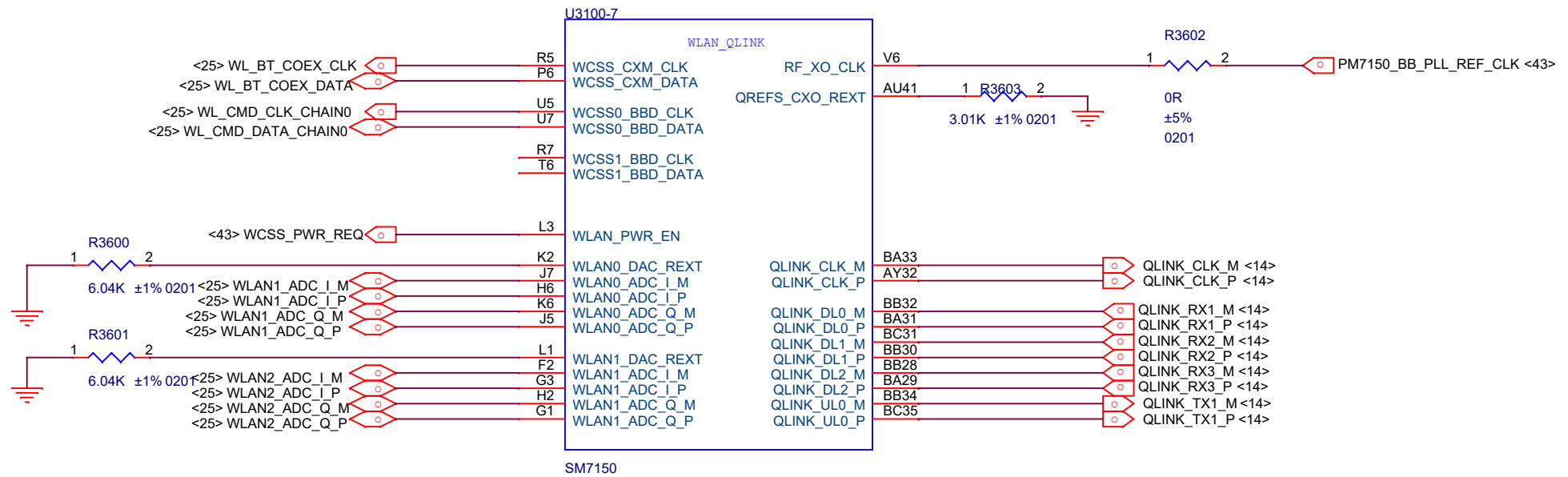
DSI0_A0_LN0_P
DSI0_B0_LN0_M
DSI0_C0_LN1_P
DSI0_A1_LN1_M
DSI0_B1_CLK_P
DSI0_C1_CLK_M
DSI0_A2_LN2_P
DSI0_B2_LN2_M
DSI0_C2_LN3_P
DSI0_NC_LN3_M

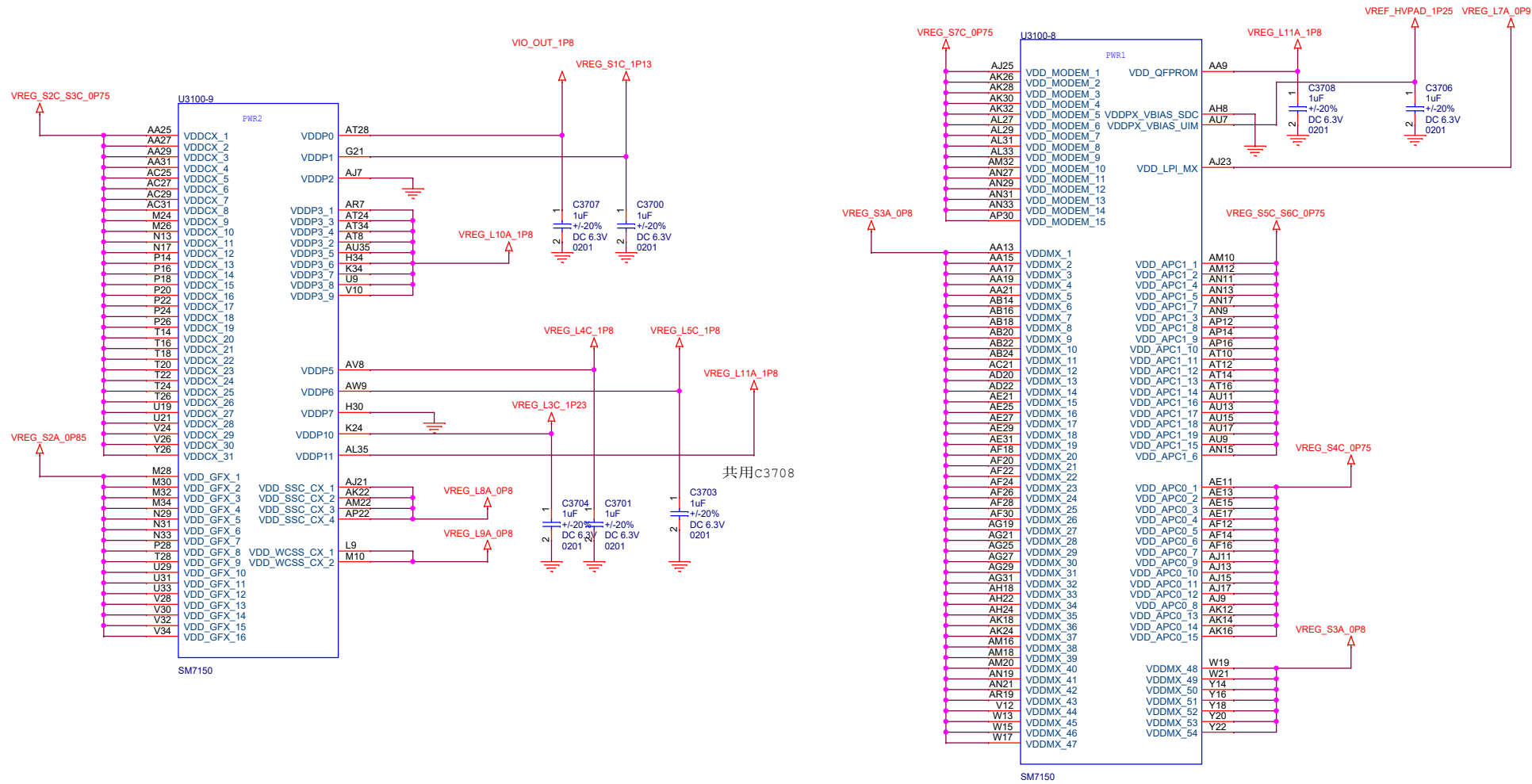
AD36
AC37
AC35
AB36
AA37
Y38
Y36
W37
W35
V36

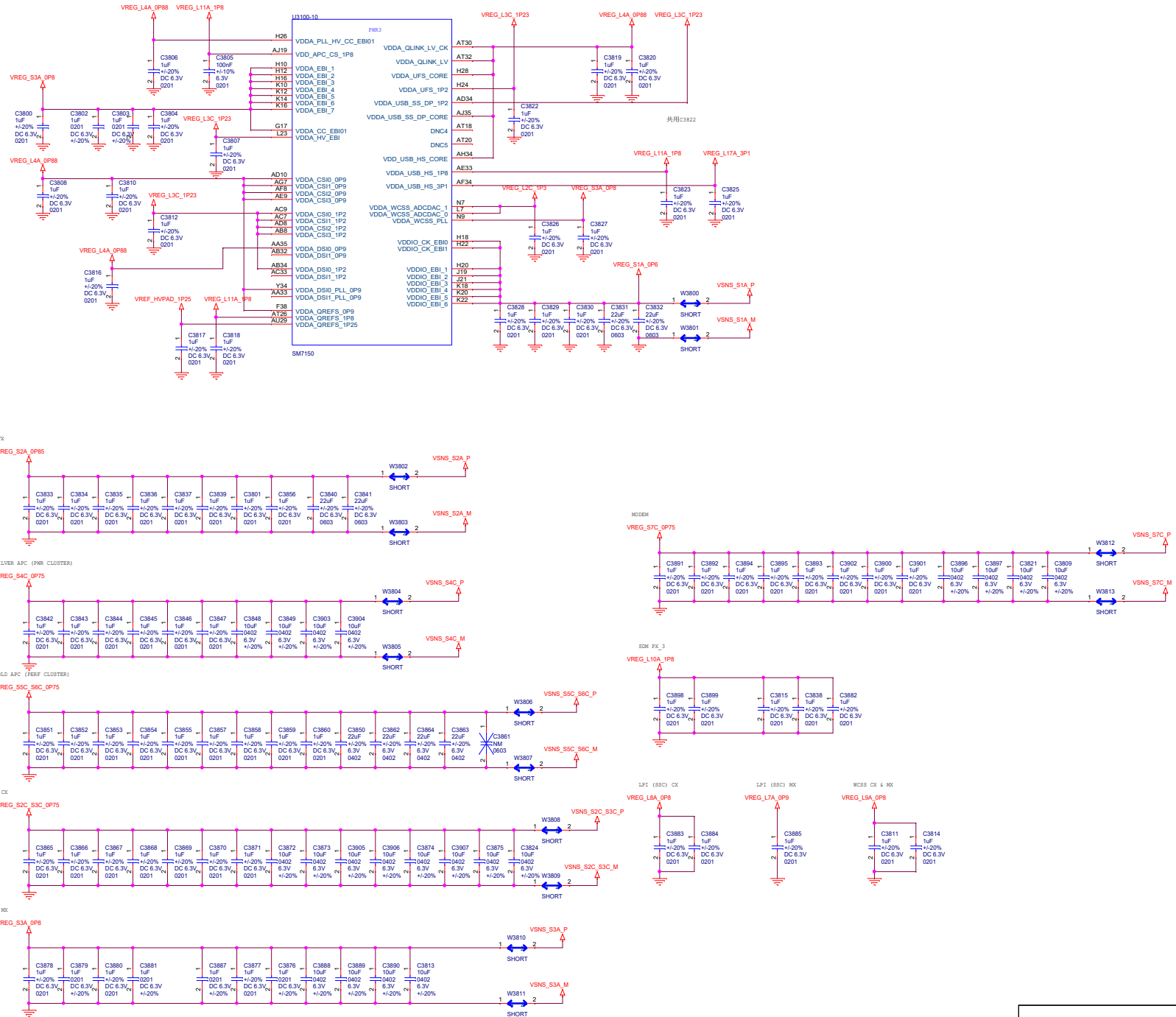
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MIPI_DSI0_CLK_P <65>
MIPI_DSI0_CLK_M <65>
MIPI_DSI0_LANE2_P <65>
MIPI_DSI0_LANE2_M <65>
MIPI_DSI0_LANE3_P <65>
MIPI_DSI0_LANE3_M <65>

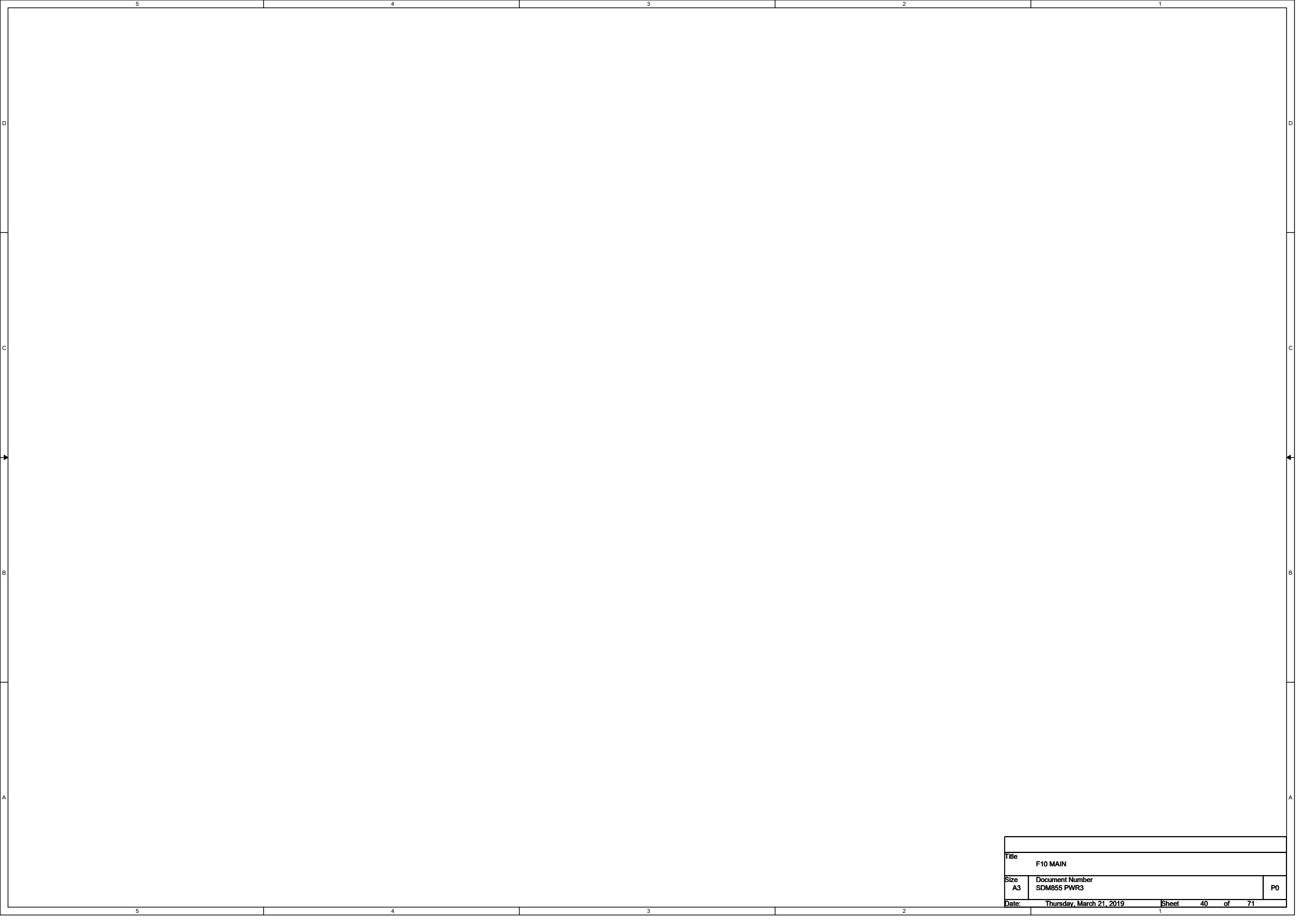
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DSI1_B0_LN0_M
DSI1_C0_LN1_P
DSI1_A1_LN1_M
DSI1_B1_CLK_P
DSI1_C1_CLK_M
DSI1_A2_LN2_P
DSI1_B2_LN2_M
DSI1_C2_LN3_P
DSI1_NC_LN3_M

AG39
AF40
AF38
AE39
AD40
AC41
AC39
AB40
AB38
AA39

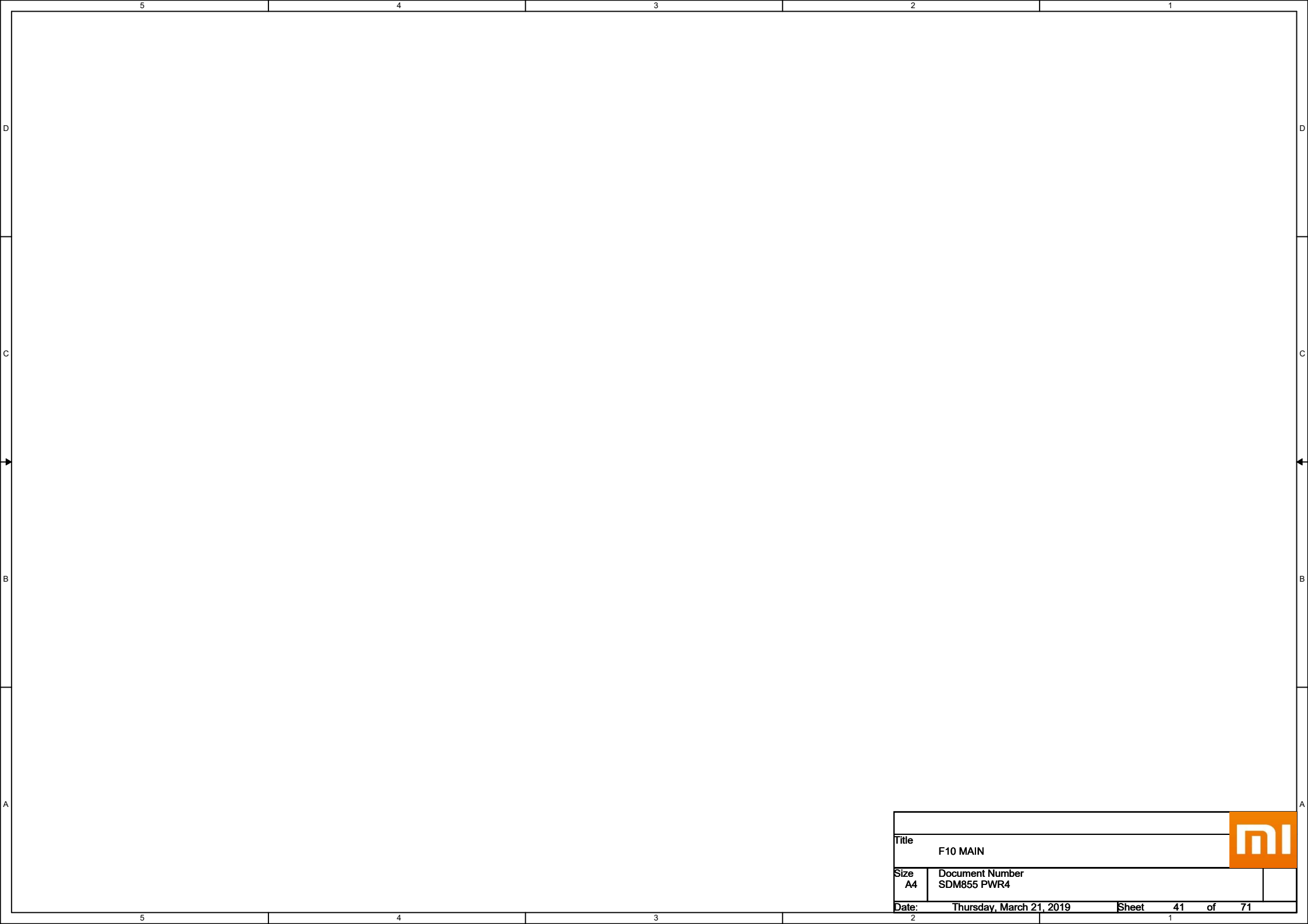




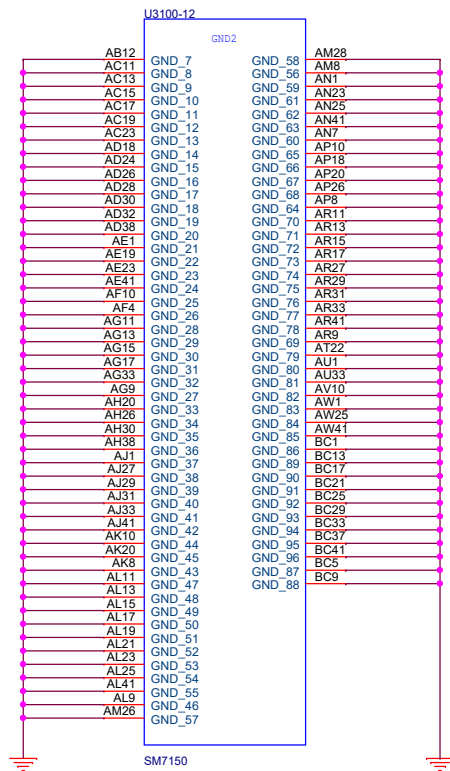
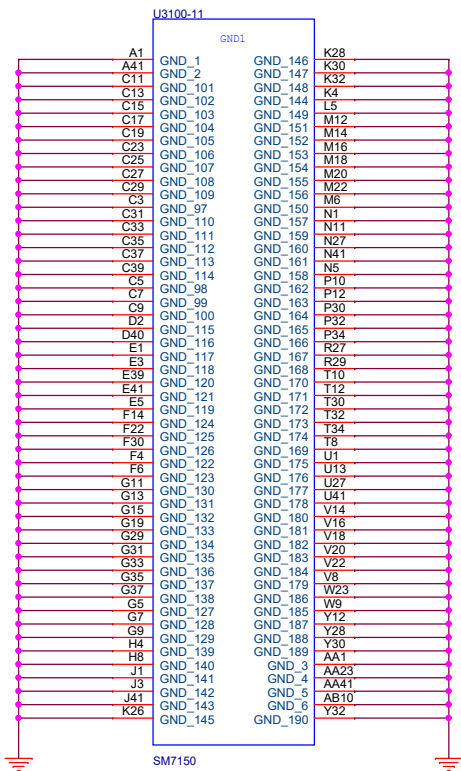


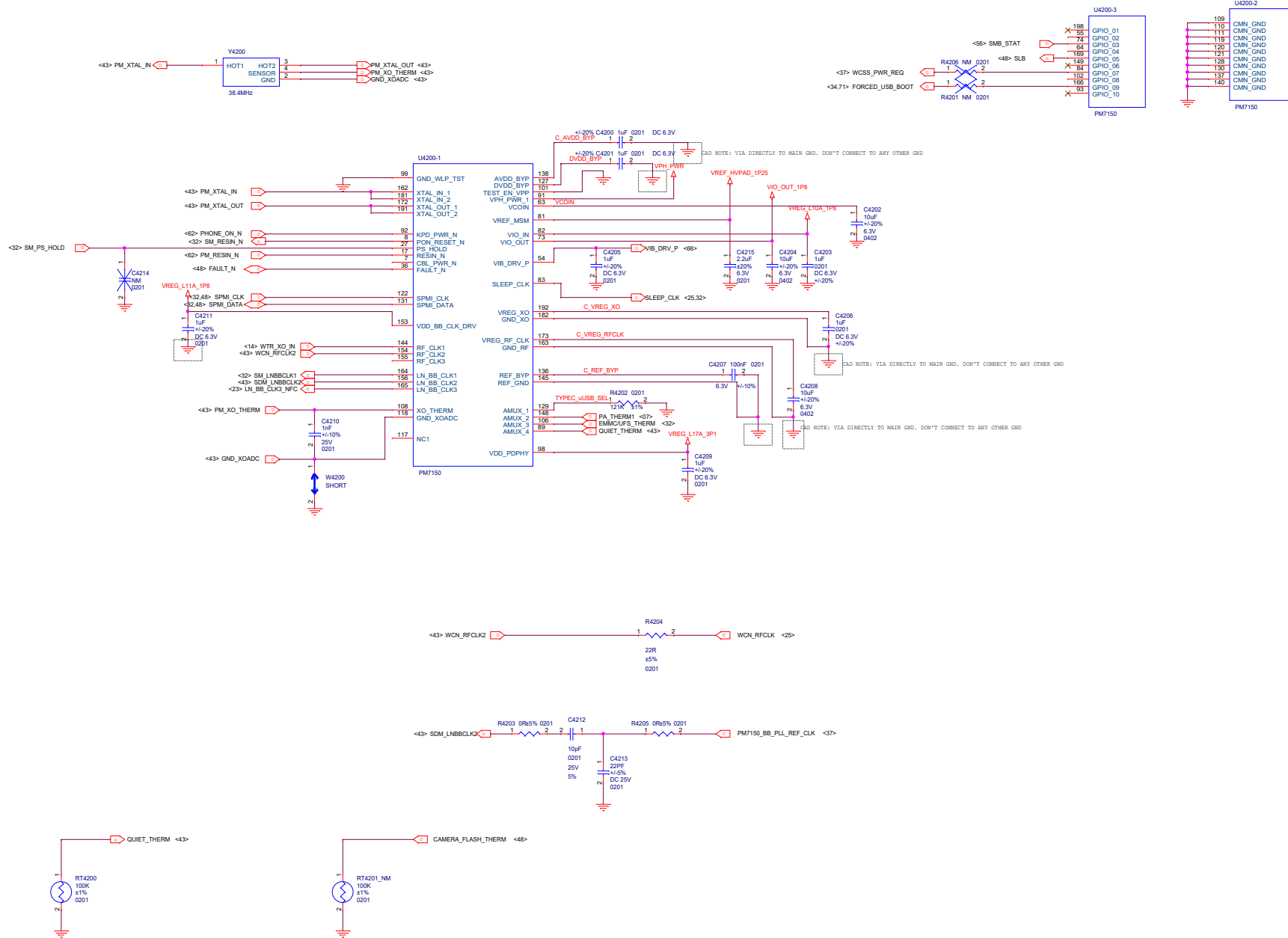


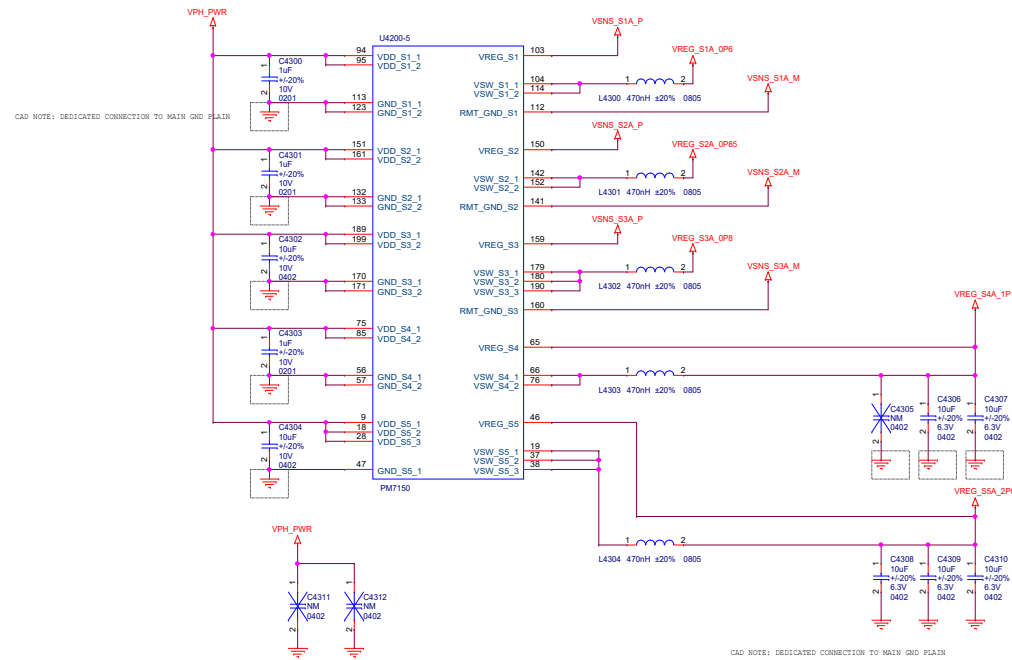
Title		
F10 MAIN		
Size	Document Number	P0
A3	SDM855 PWR3	
Date:	Thursday, March 21, 2019	Sheet 40 of 71

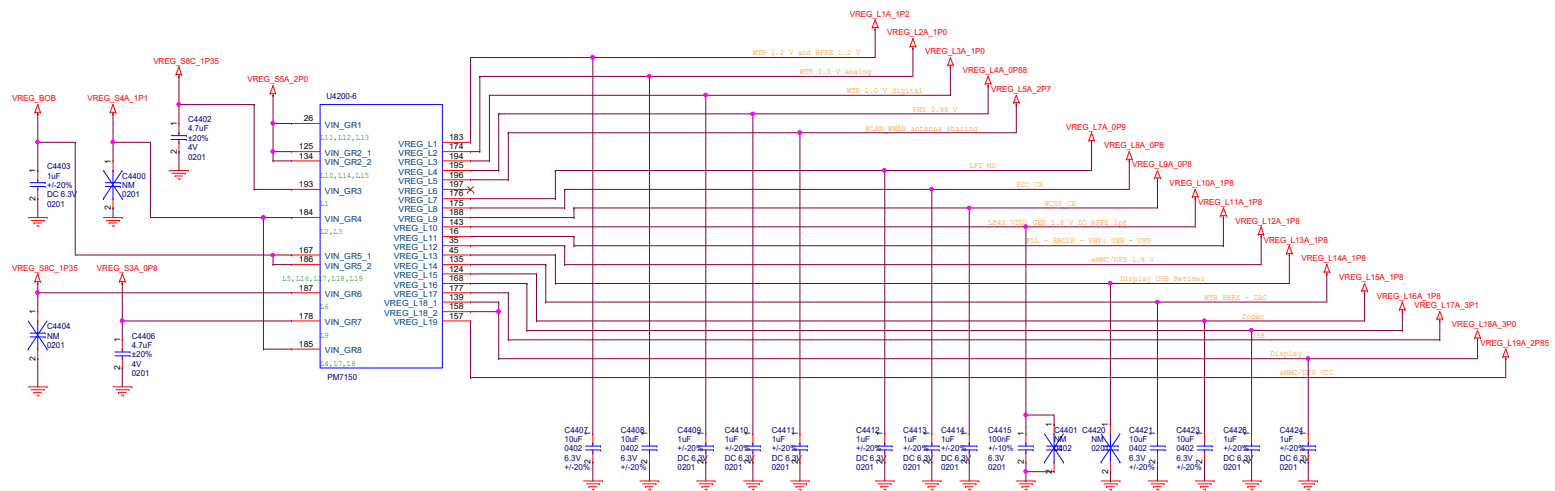


Title		F10 MAIN	
Size	A4	Document Number	SDM855 PWR4
Date:		Thursday, March 21, 2019	Sheet 41 of 71



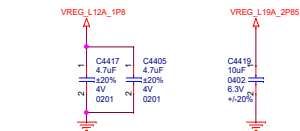


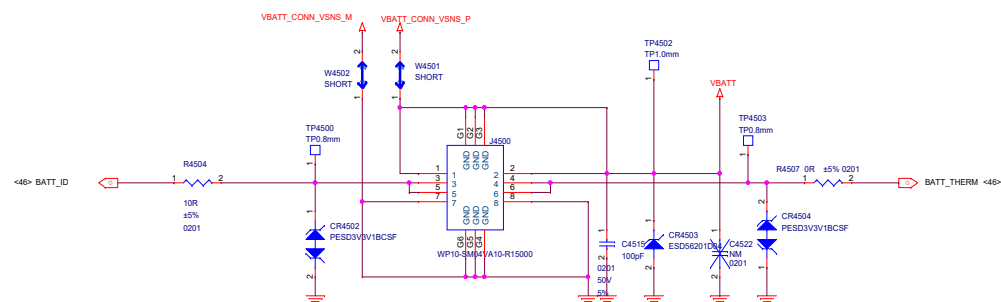
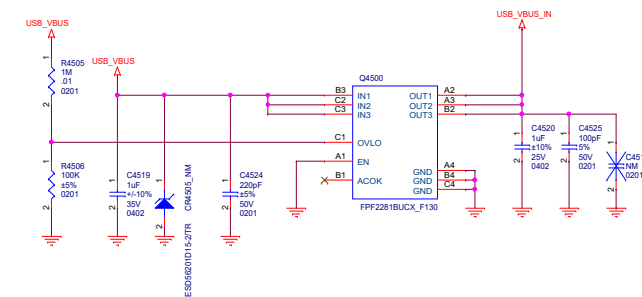




VREG_L11A_1P8预留电容删除

PSEUDO CAPLESS LDOs
For CAPLESS LDOs: If decaps on the load side do not
add up to LDO spec, then install the cap close to the PMIC

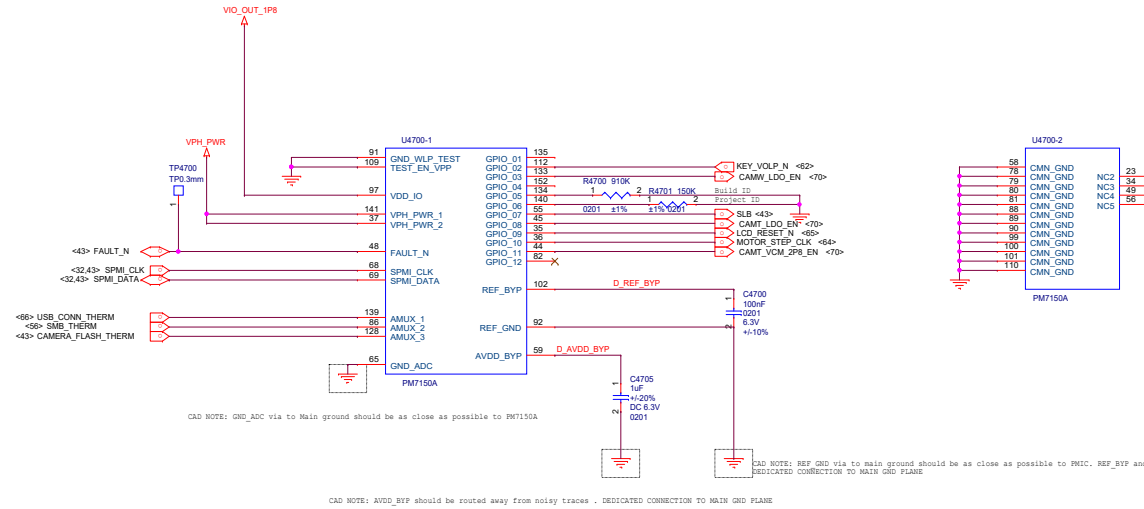
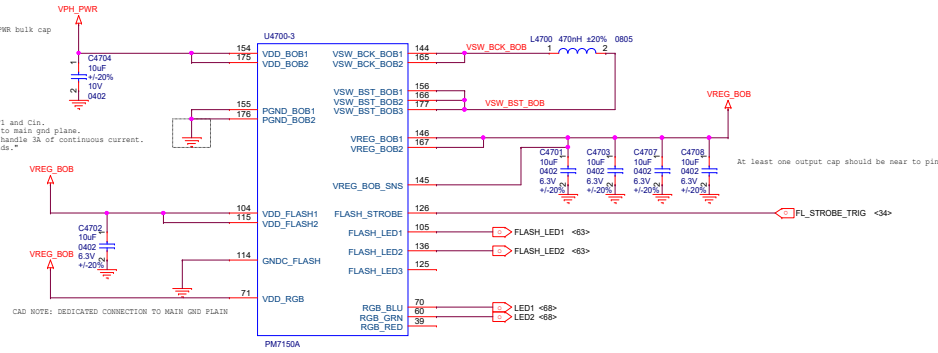


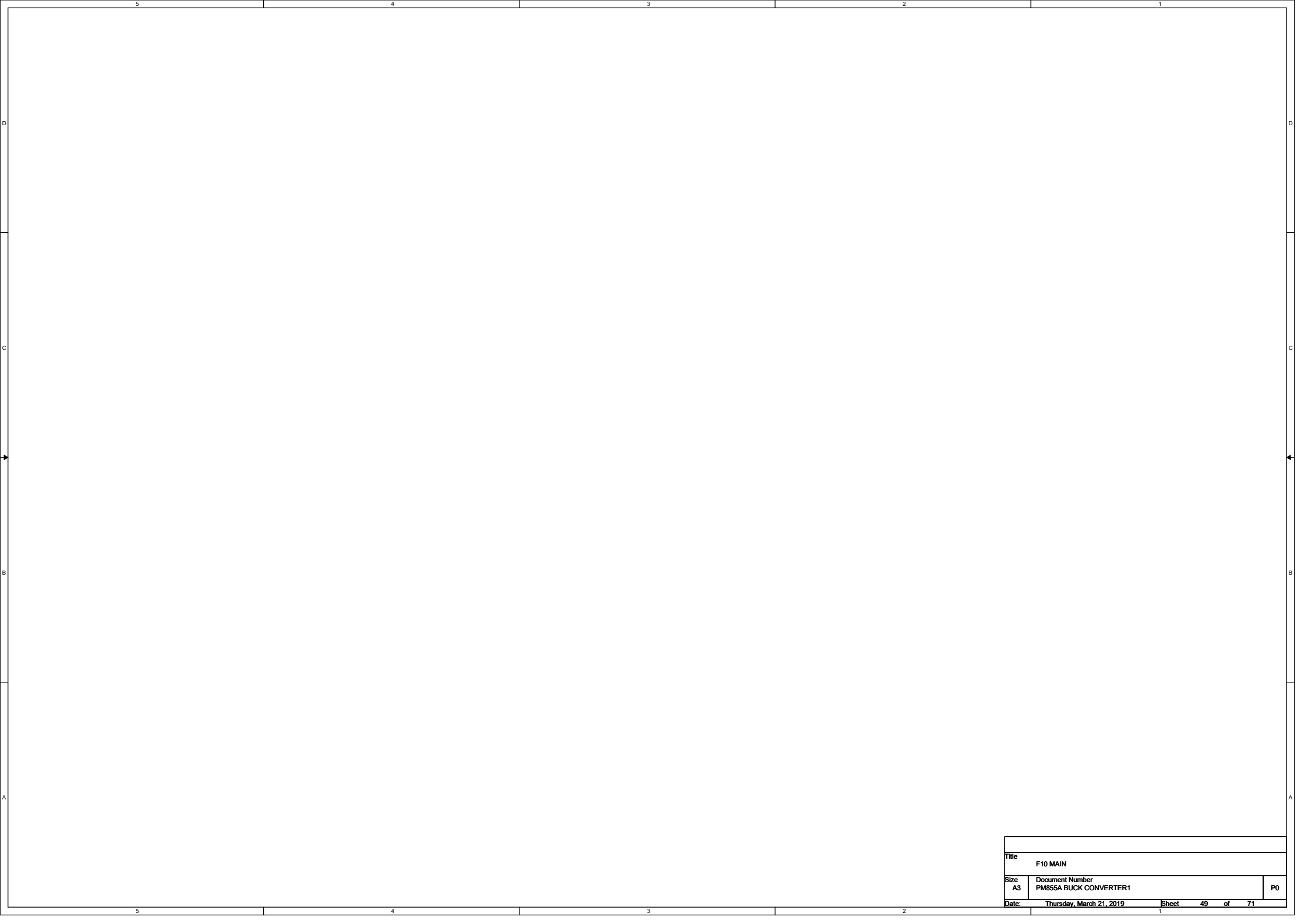


Title F10 MAIN			
Size A2	Document Number PM855 LDCs		
Date: Thursday, March 21, 2019		Sheet 46	of 71

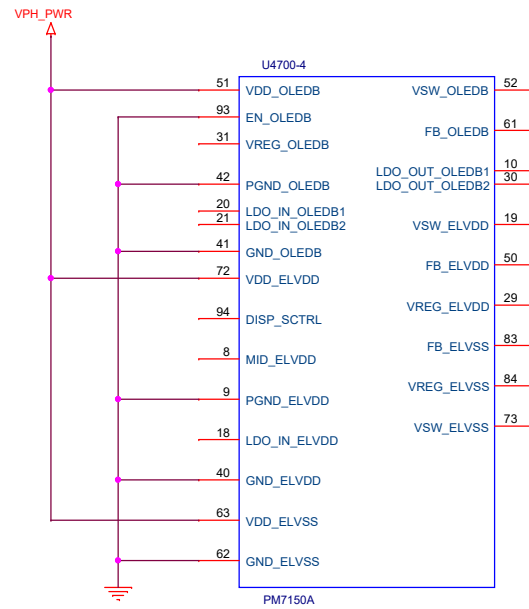
CAD Note: Place C4704 right next to the PMIC. This also acts as VPH_PWR bulk cap

CAD NOTES: Layout Note: PGND_BOB
"Dedicated trace from pin to C0001 and Cln.
Dedicated via from cap directly to main gnd plane.
Trace and via should be able to handle 3A of continuous current.
Do NOT connect to any other grounds."





Title		
F10 MAIN		
Size	Document Number	P0
A3	PM855A BUCK CONVERTER1	
Date:	Thursday, March 21, 2019	Sheet 49 of 71



D

D

C


C

B

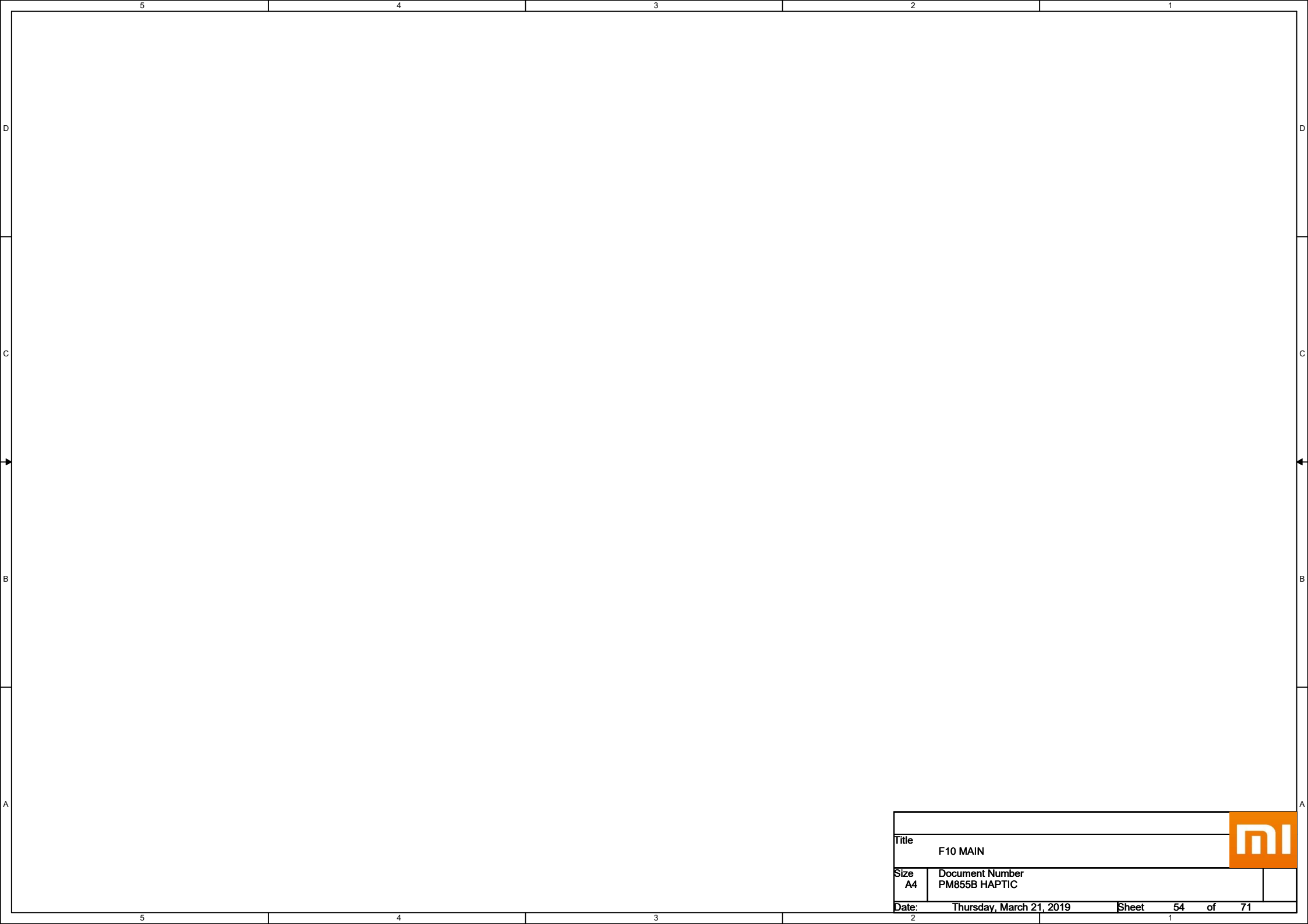
B


A

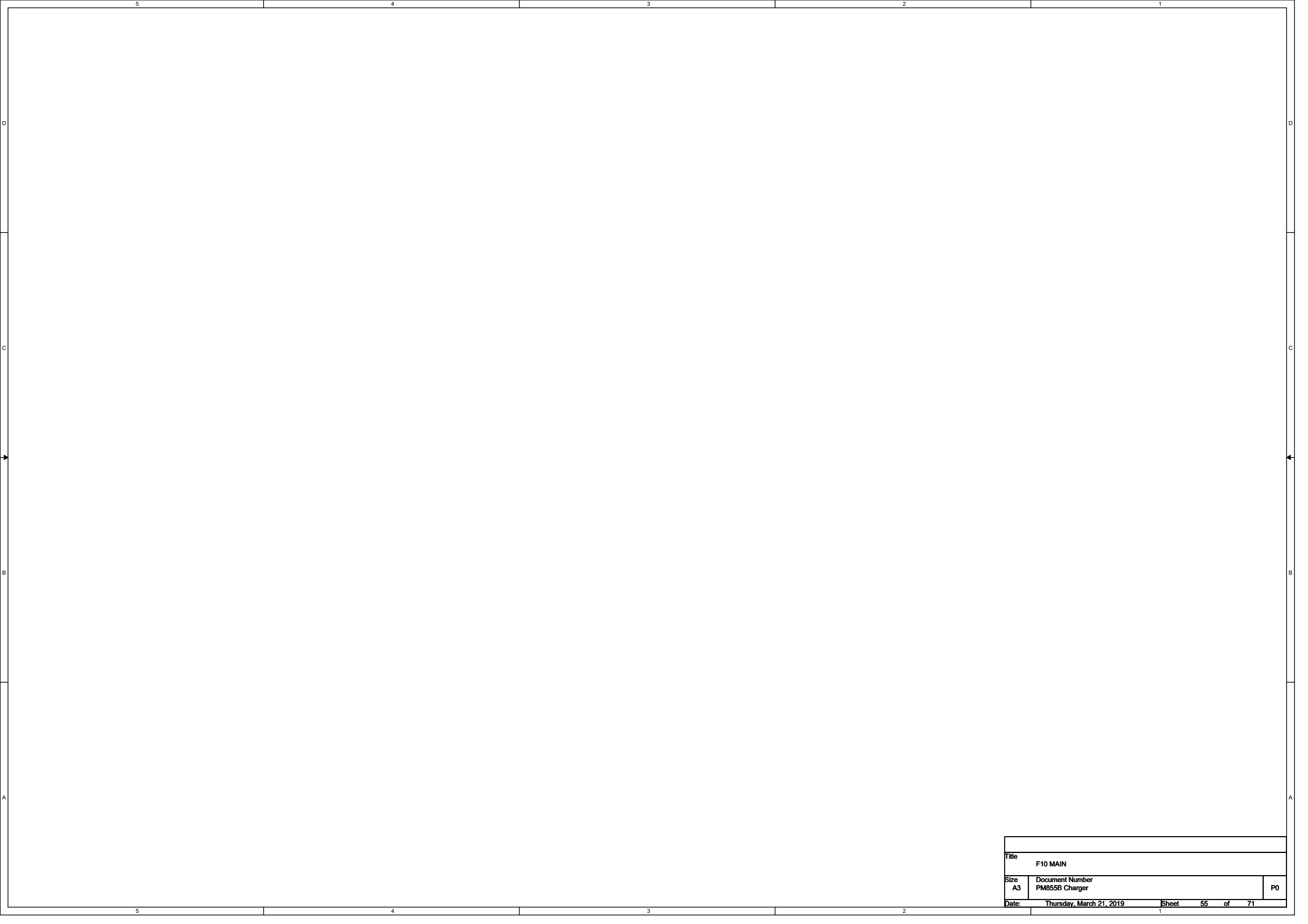
A

			
Title F10 MAIN			
Size A4	Document Number PM855A LDOs		
Date:	Thursday, March 21, 2019	Sheet	52 of 71



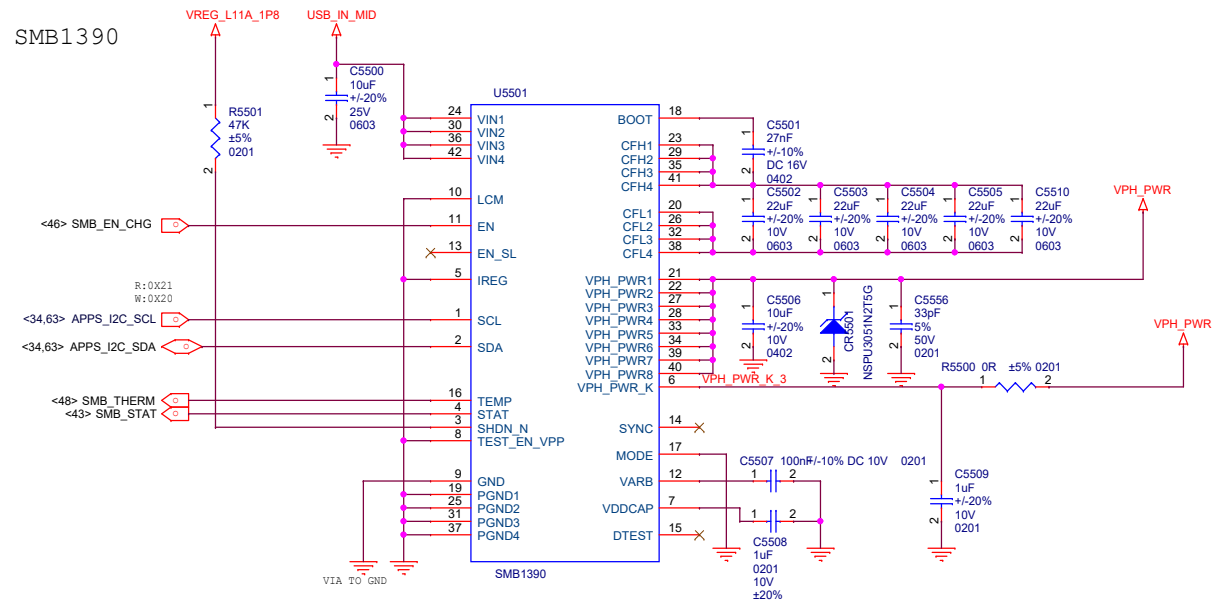


Title		F10 MAIN		
Size	A4	Document Number	PM855B HAPTIC	
Date:		Thursday, March 21, 2019		Sheet 54 of 71

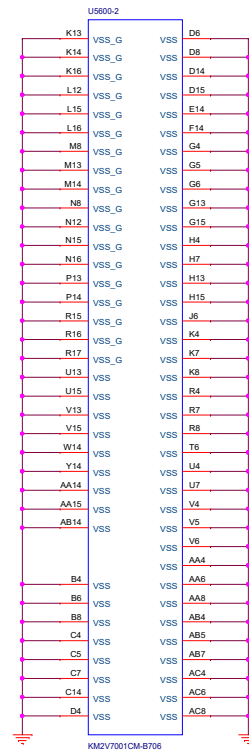
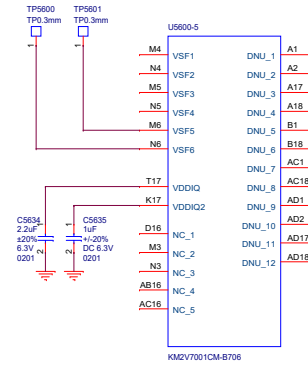
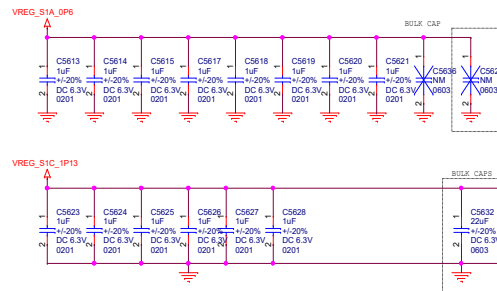
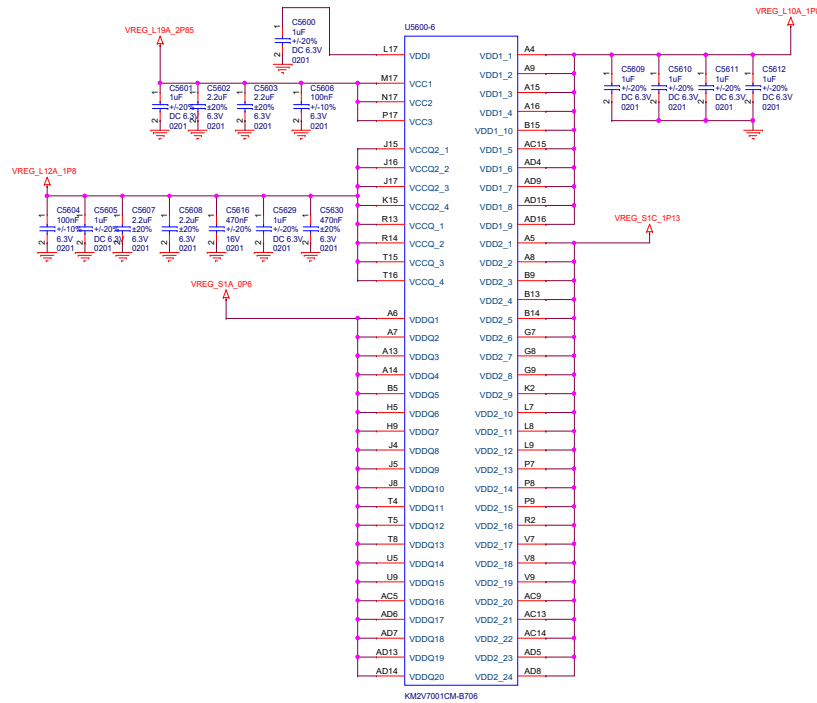


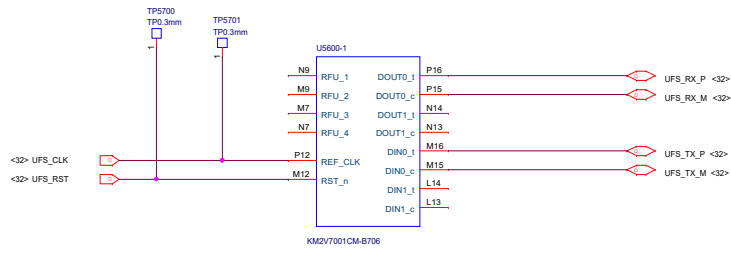
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F10 MAIN		
Size	Document Number	P0
A3	PM855B Charger	
Date:	Thursday, March 21, 2019	Sheet 55 of 71

SMB1390

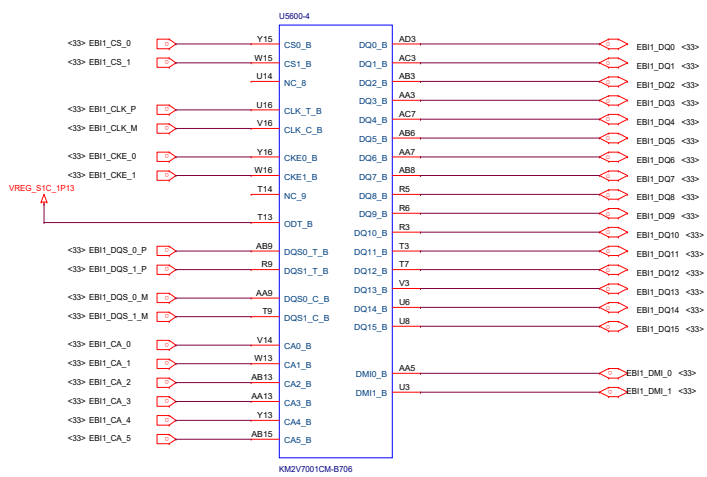
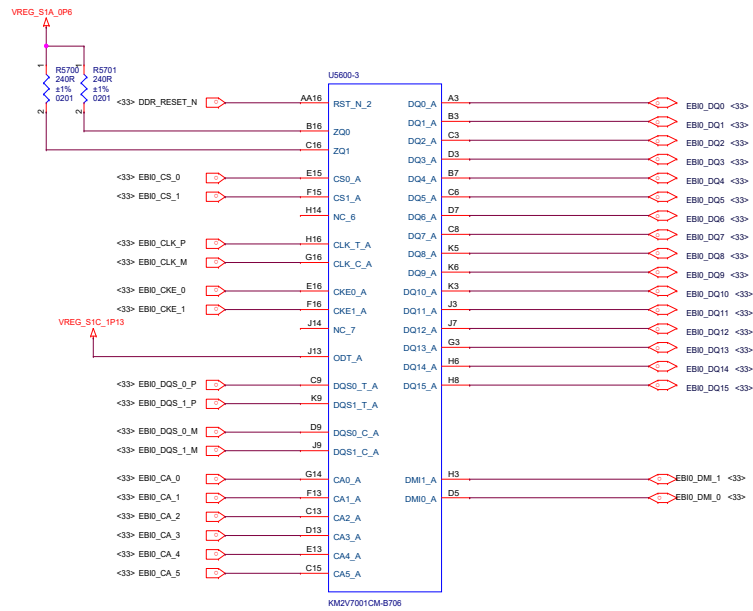


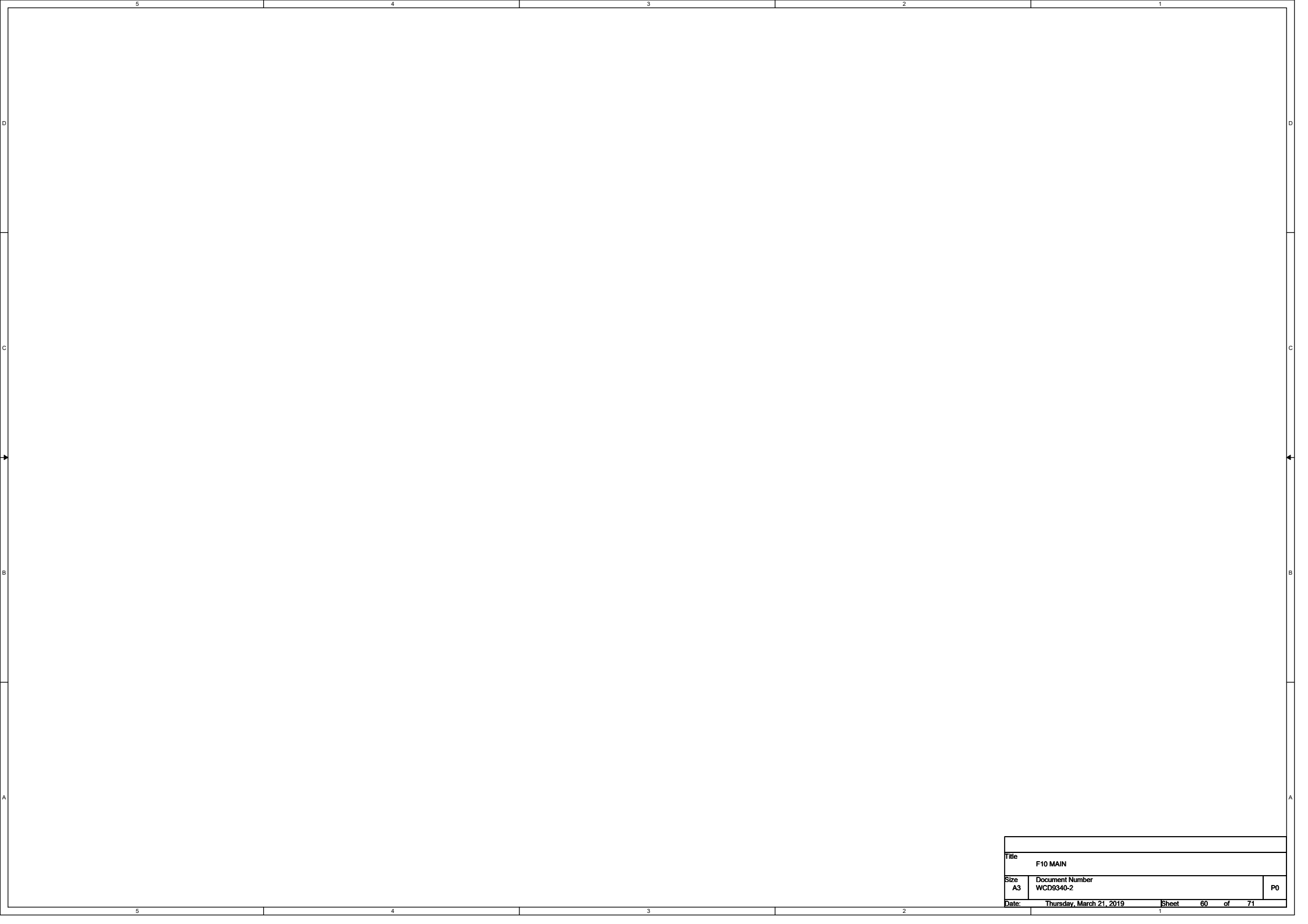
Title		
F10 MAIN		
Size	Document Number	P0
A3	SMB1390&WL POWER	
Date:	Thursday, March 21, 2019	Sheet 56 of 71



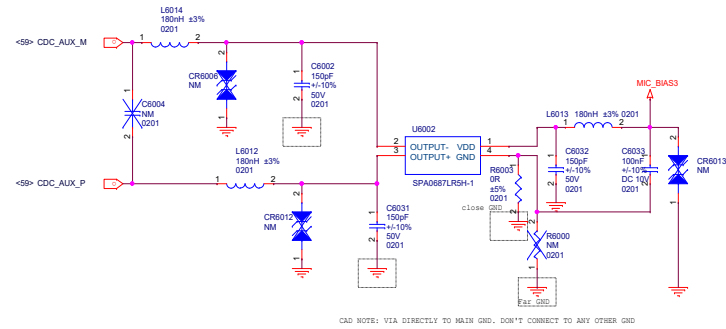


LPDDR4 / 4x





AUX MIC

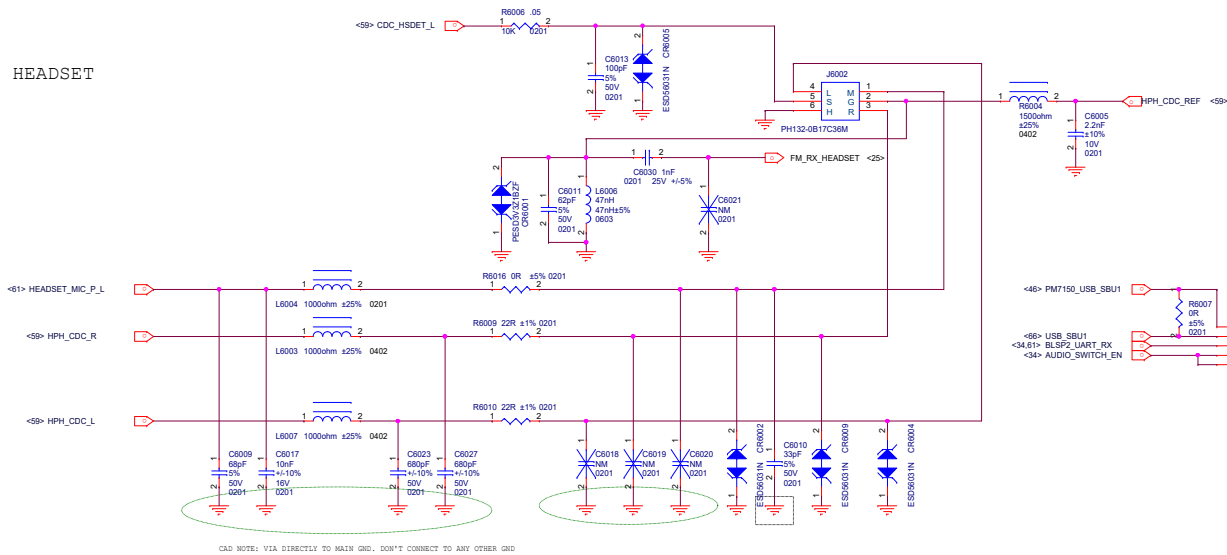


AUX MIC

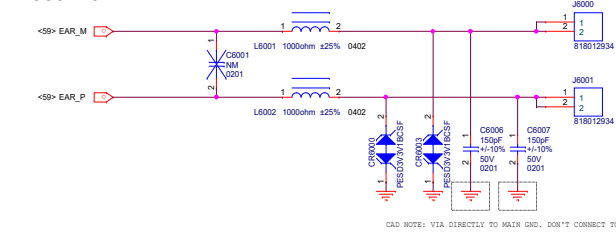
UART SWITCH



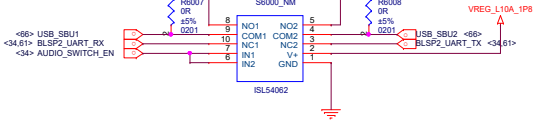
HEADSET



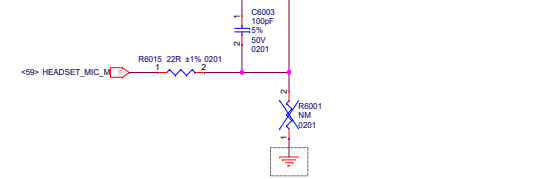
Receiver



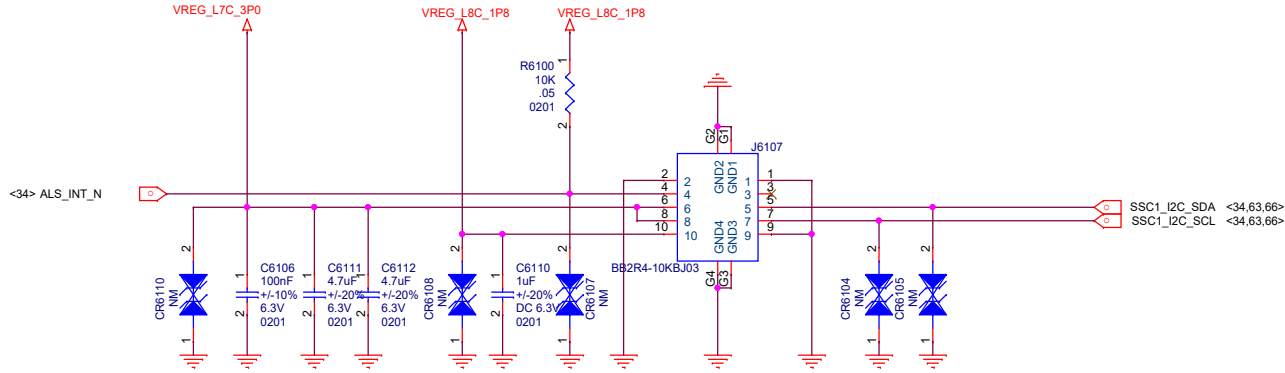
PM7150_USB_SBU1



HEADSET_MIC_P

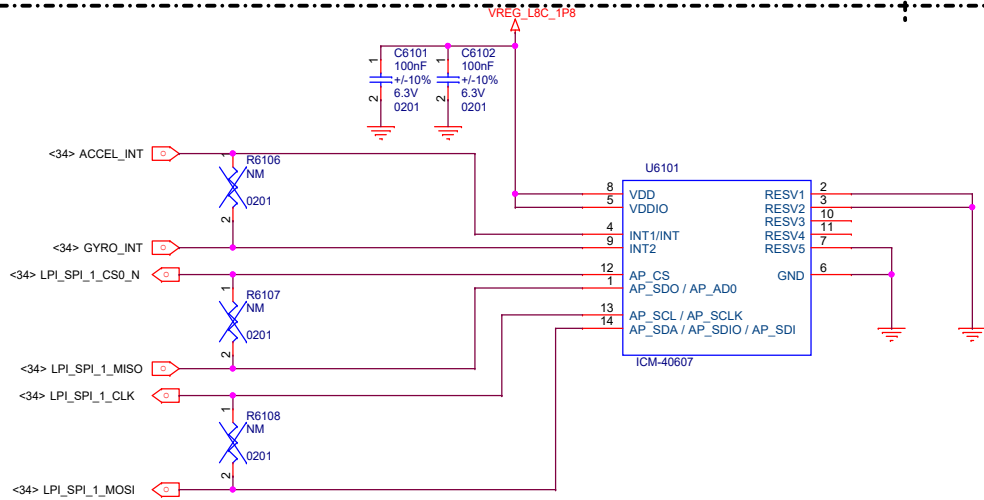


P-sensor

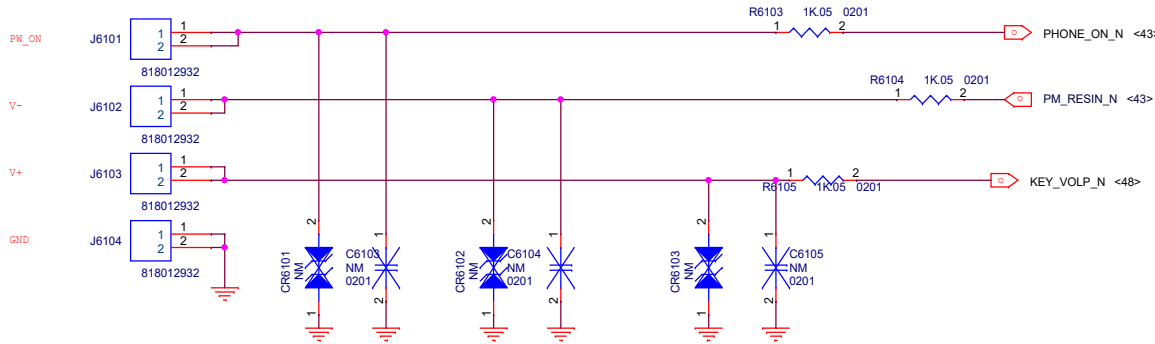


L-sensor

A+G

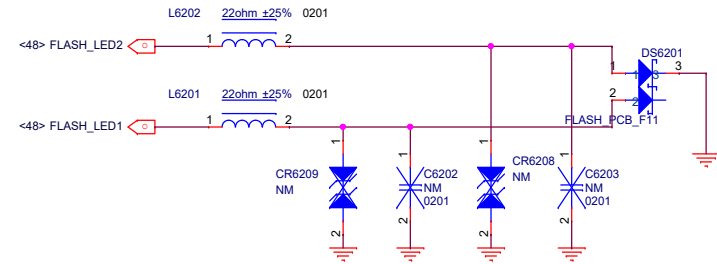
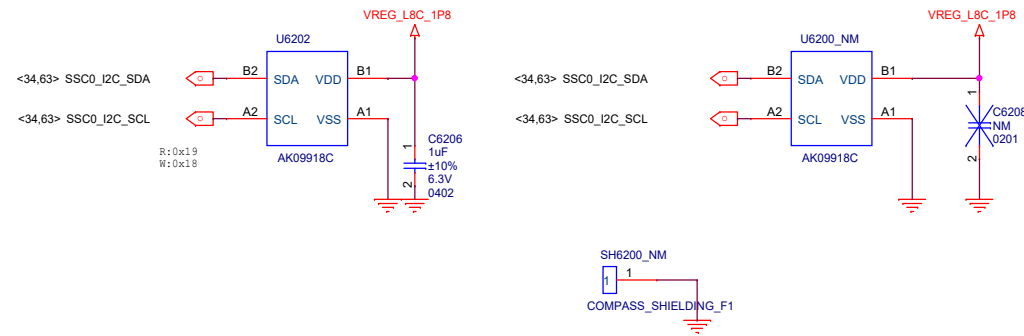


Sidekey

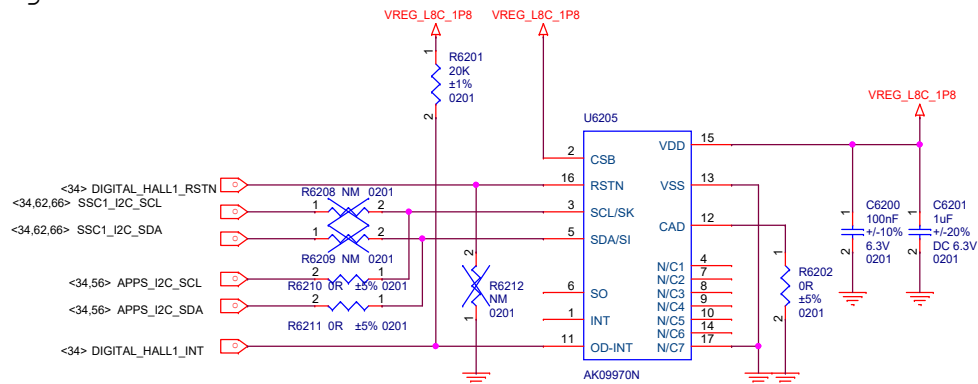


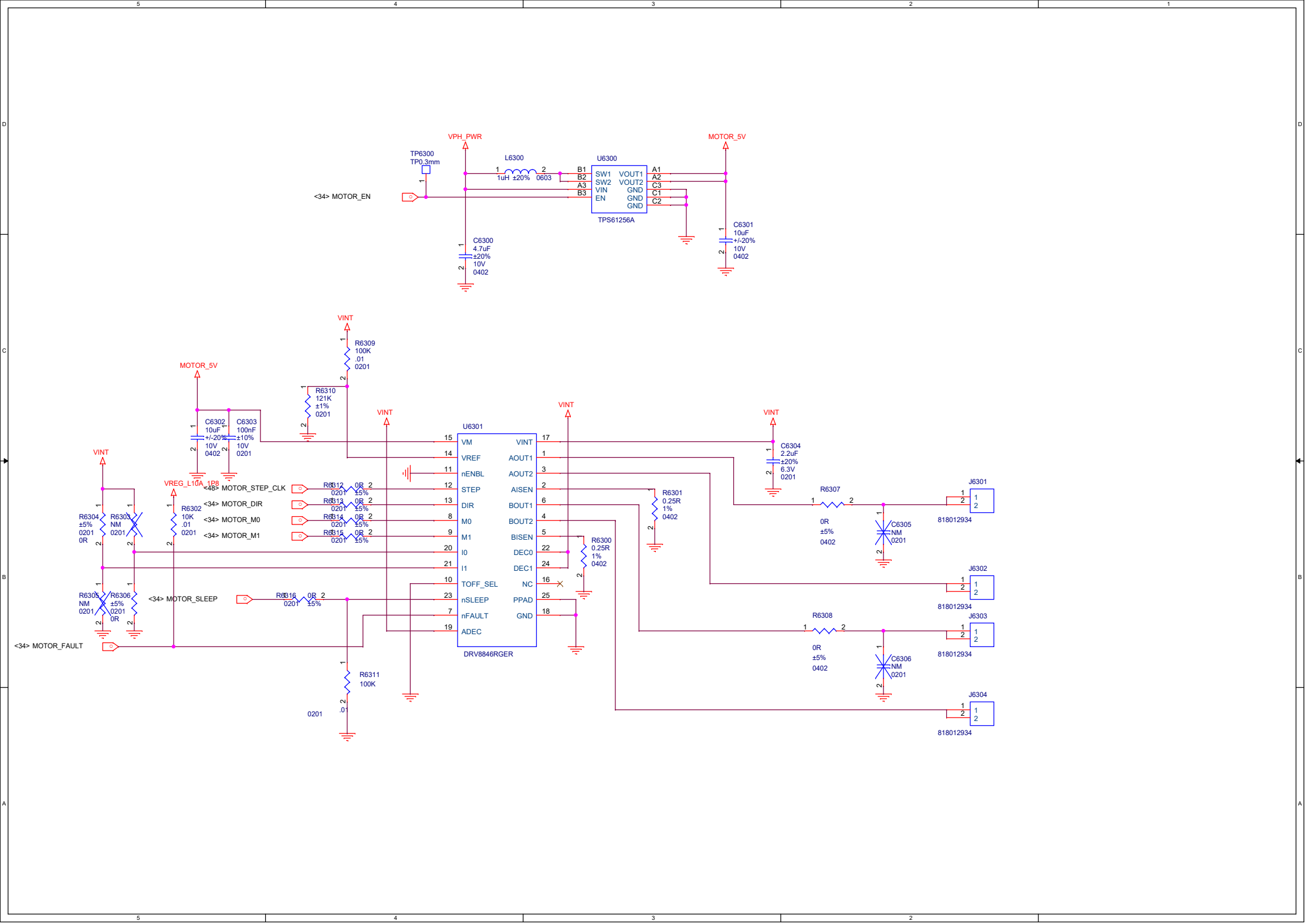
FingerPrint to SUB board

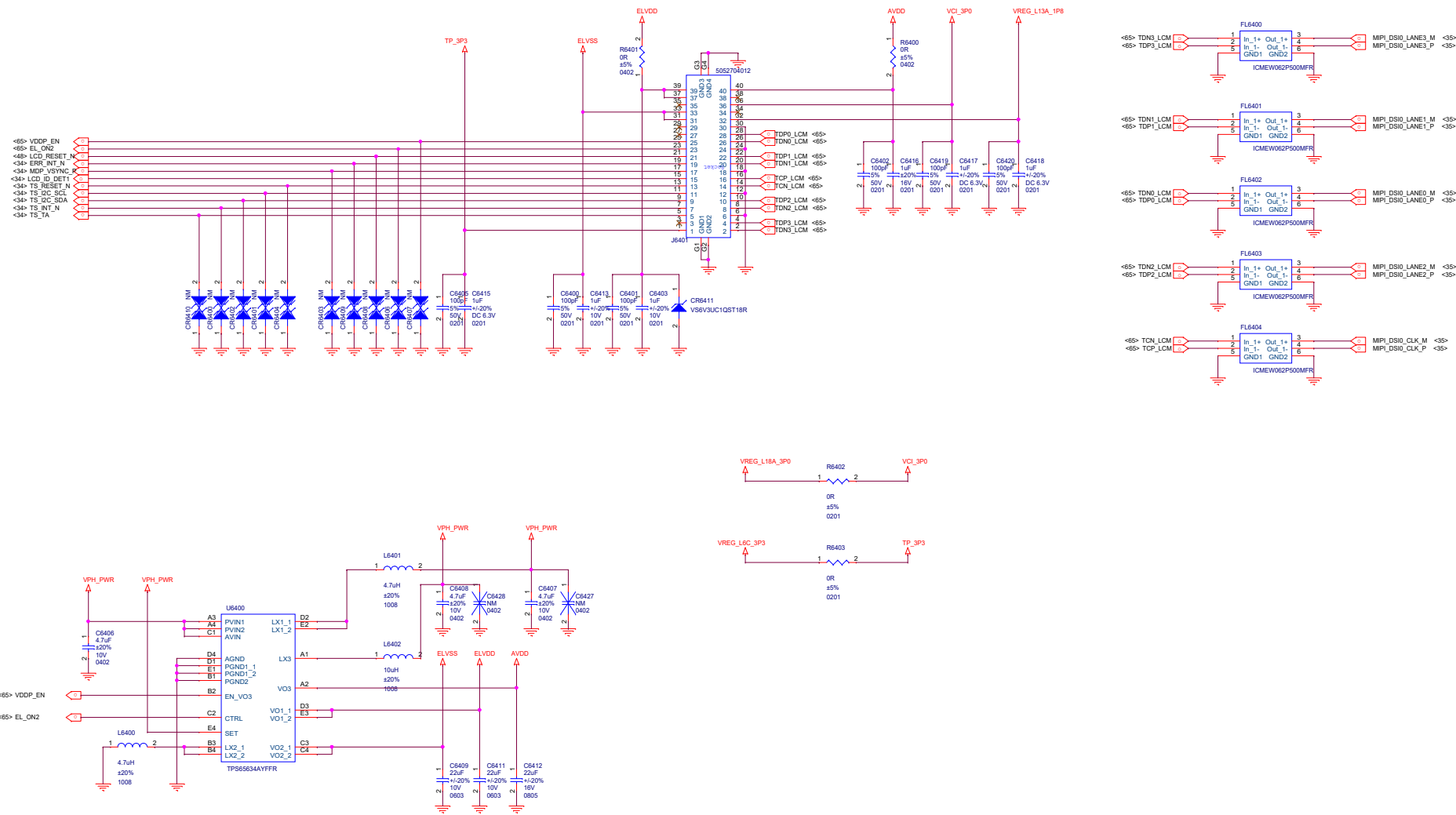
COMPASS

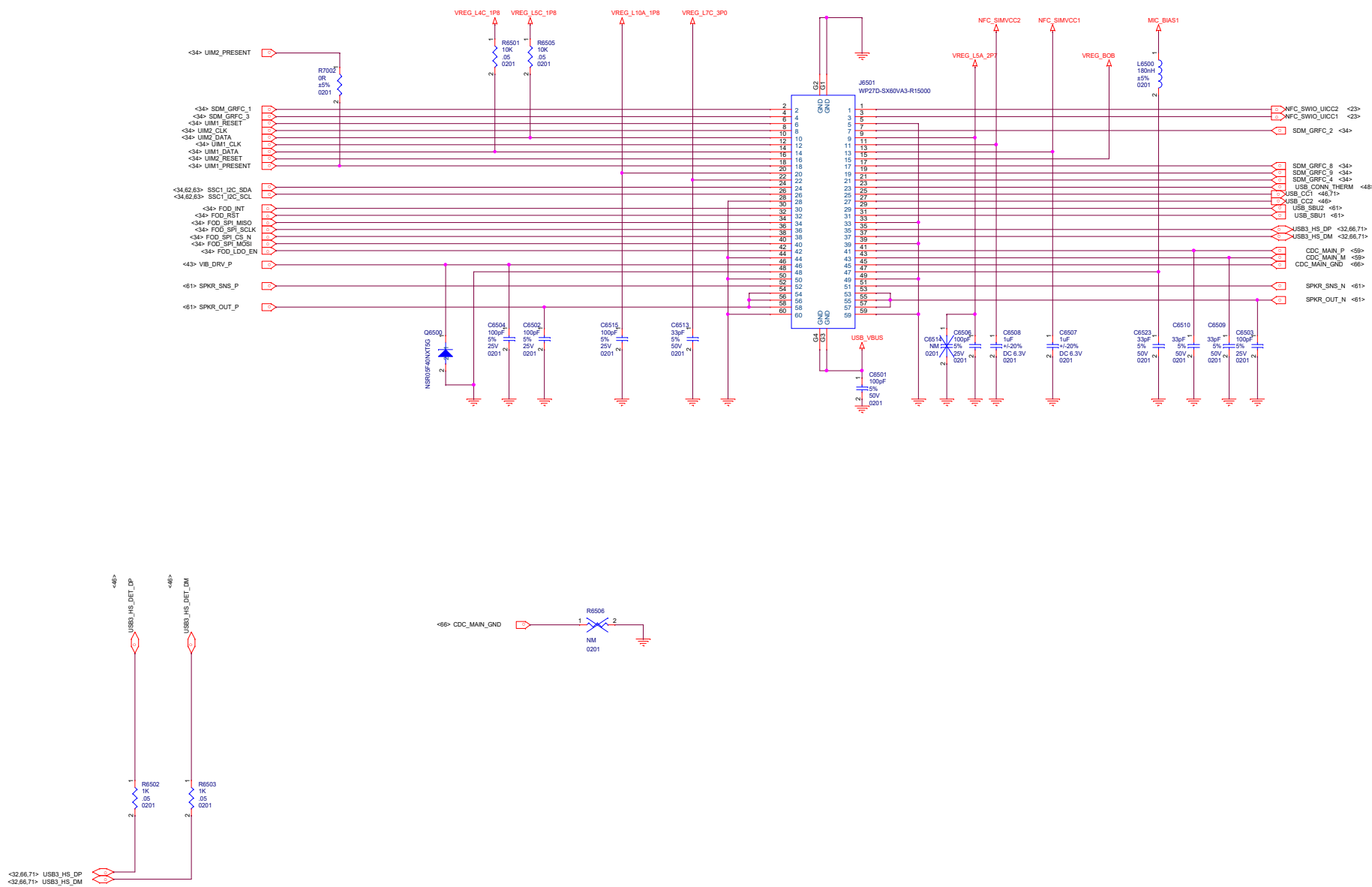


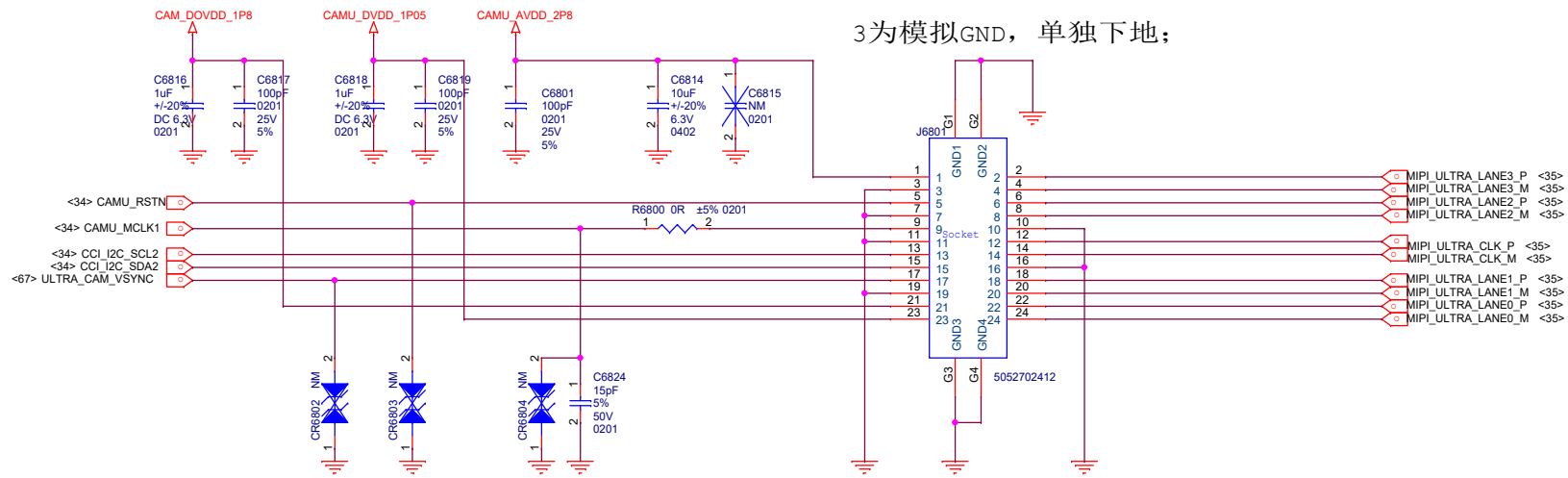
Digital HALL



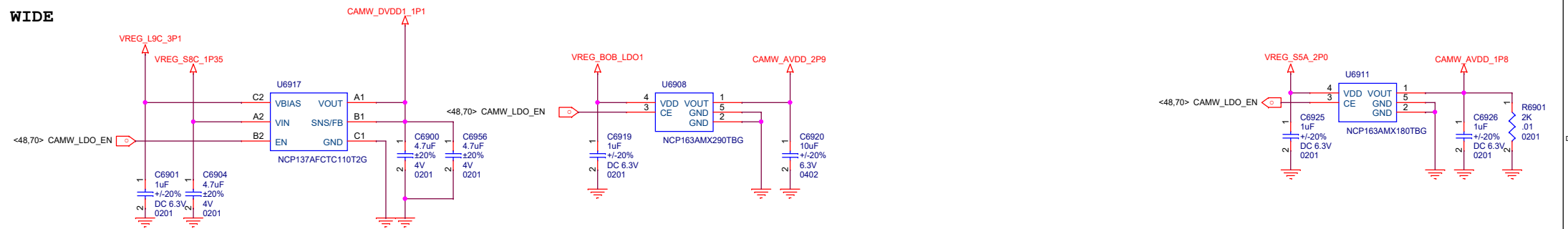




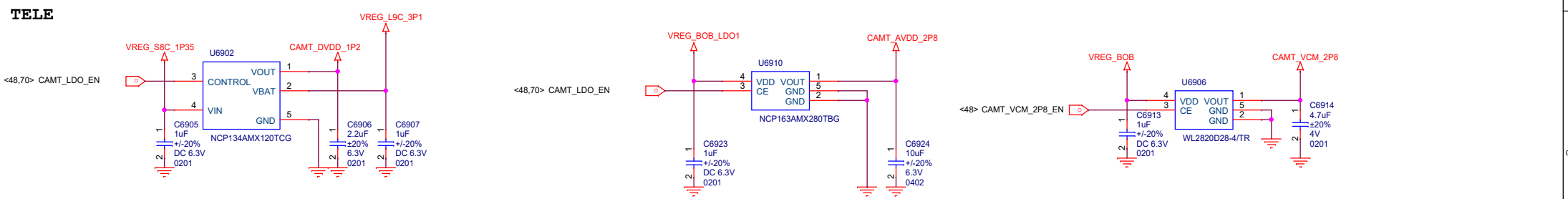




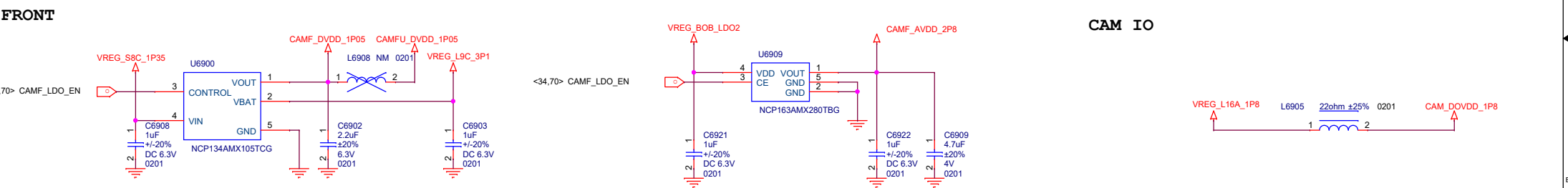
WIDE



TELE



FRONT



CAM IO



ULTRA

